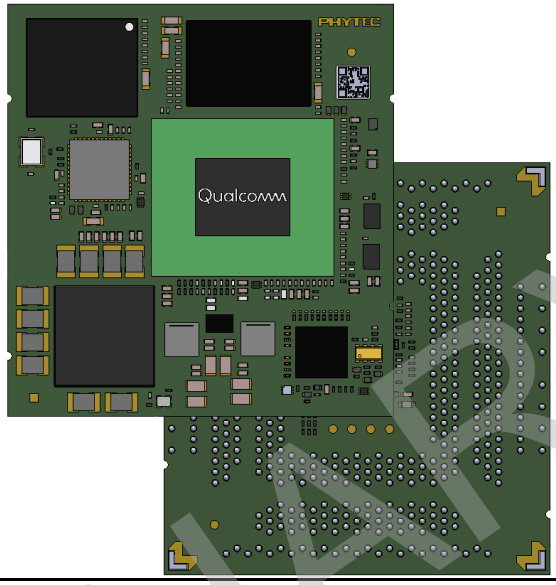
PHYTEC Datasheet | phyFLEX®-IQ2390 System on Module (SOM)

PFL-G-08 | PCB 1650.0

Table of Contents

Table of Contents 1
1 Specifications 2
1.1 Block Diagram 2
1.2 Features 3
1.3 Orderable Part Numbers 4
1.4 Pinout Table 4
1.5 Physical Dimensions 15
1.6 Technical and Electrical Specifications 16
2 Revision History 17



Description

The phyFLEX®-IQ23 is a compact, high-performance System on Module engineered around the powerful Qualcomm® Dragonwing™ IQ2390, designed to deliver exceptional compute and machine learning capabilities to the industrial edge. Its heterogeneous architecture features a primary Arm Cortex-A78 core running at up to 1.9 GHz paired with three Cortex-A55 efficiency cores at 1.8 GHz, alongside a dedicated RISC-V SiFive E61 MCU for real-time, low-latency processing tasks. To accelerate complex multimedia and vision workloads, the module integrates an Adreno™ 704 graphics accelerator and a Hexagon™ V66 AI core capable of 1.1 TOPS of inferencing performance. This robust compute foundation makes it an ideal platform for edge AI, embedded vision systems, and advanced industrial controllers that require responsive, localized data processing and secure application execution backed by the Qualcomm® Trusted Execution Environment, a hardware-supported KeyStore, and Arm TrustZone®.

Built for versatile connectivity and environmental resilience, the phyFLEX-IQ23 supports dual 4-lane MIPI CSI camera inputs and flexible display routing via either a 4-lane LVDS or MIPI-DSI interface. The module provides extensive high-speed I/O, including a PCIe Gen2 lane, USB 3.1, USB 2.0, and 10 Qualcomm Universal Peripheral (QUP) blocks for customizable serial interfaces. Industrial networking is supported by dual Gigabit Ethernet interfaces with Time-Sensitive Networking (TSN), one utilizing an on-board PHY and the second brought out via RGMII. All this capability, backed by up to 16 GB of LPDDR4x memory, up to 128 GB of eMMC storage, and a 32 KBit EEPROM, is delivered in a future-proof 48 mm × 45 mm FPSC footprint. Operating from a single 5V supply and rated for temperatures from -30°C to +85°C, the phyFLEX-IQ23 provides a highly integrated, production-ready foundation for rugged and space-constrained embedded designs.

- Up to 16GB LPDDR4X RAM
- Up to 128GB on-board eMMC
- 1x Gigabit Ethernet PHY (signals brought out to connector as differential pairs)
- 2x 4KB I^2C EEPROM (one for customer use and one for PHYTEC's use)
- 1x On-board RTC
- 537 Pin FTGA footprint: An FPSC size M footprint

PRELIMINARY

1 Specifications

1.1 Block Diagram

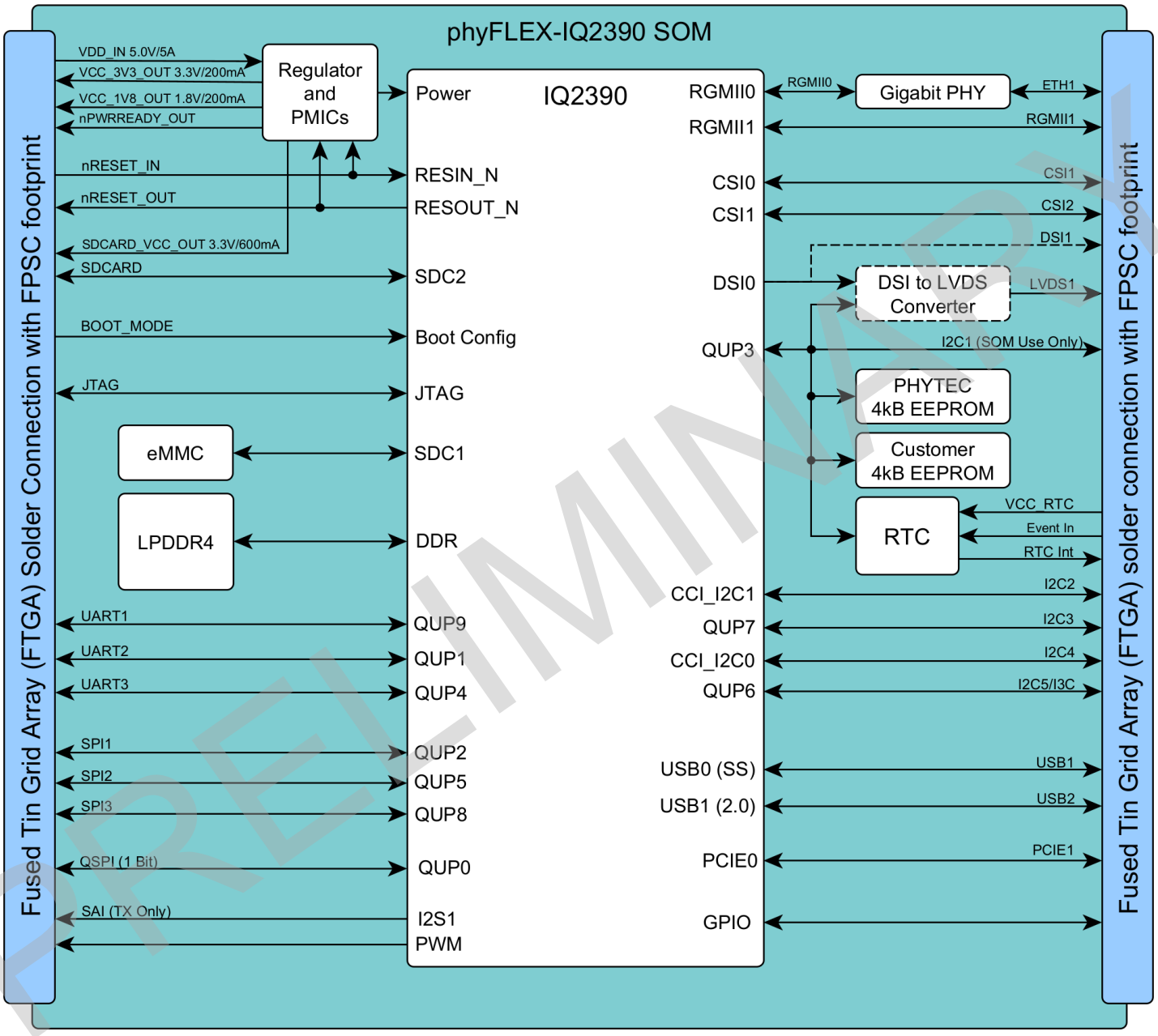


Figure 1. phyFLEX-IQ23 Block Diagram

1.2 Features

PROCESSOR	
Processor	Qualcomm IQ2390
Architecture	Arm Cortex A78 / 3x A55
Frequency	1.9 GHz / 1.8 GHz
Co-Processors	SiFive E61 RISC-V MCU at 600 MHz
AI/DSP	Qualcomm® Hexagon™ v66A compute Digital Signal Processor (cDSP)
MEMORY	
RAM	2GB default, 16GB LPDDR4X max
eMMC	32 GB default / 128 GB max
EEPROM	2x 4KB I2C
SD/SDIO/MMC Interfaces	1
HIGH-SPEED INTERFACES	
USB	1x 3.1 Dual Role, 1x 2.0 Dual Role
PCIe	PCIe Gen 2
PERIPHERALS	
I3C	1
GPIO	120
I2C	10x I2C, 2x dedicated camera I2C
PWM	15
SPI	7
UART	9
CONNECTIVITY	
Ethernet	1x 1Gb, 1x RGMII
MULTIMEDIA	
Audio	4x I2S, 1x SWR, 2x DMIC
Camera	2x MIPI CSI-2
Display	1x OLDI/LVDS, 1x MIPI-DSI (not simultaneously supported)
Graphics	3D GPU (Adreno 704 at 845 MHz)
Video	1080p @ 30 fps
Wireless	1x WLAN
MISCELLANEOUS	
JTAG	Yes
RTC	Yes
Security Accelerators	Secure boot, secure debug, secure key provisioning, TrustZone, Qualcomm® Trusted Execution Environment, hardware-supported KeyStore
BOOT SOURCES	

PRELIMINARY

SD-Card	SDC2
eMMC	SDC1
USB/DFU	USB0
MECHANICAL	
Connector	537 Pin FTGA footprint
Dimensions	45mm x 48mm
OPERATING CONDITIONS	
Operating Temperature	-30° to +85° C
Power (Under Load)	TBD
Power (Typical)	TBD
Supply Voltage	5V
Note: Some of the features listed are not available simultaneously due to the multiplexing options of the various processor pins. Refer to the hardware manual for further information on available multiplexing options and section 1.4 of this datasheet for the pinout of signals.	

1.3 Orderable Part Numbers

TBD

Table 1 phyFLEX-IQ23 Orderable Part Numbers

Part Number	Description	Configuration Details (SOC / LPDDR4 / eMMC / Flash / Ethernet PHY / RTC / Temp)
Custom Configurations Available	Contact sales@phytec.com	

1.4 Pinout Table

Table 2 phyFLEX-AM62Px Connector X1, Mandatory/Optional Pinout

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
L24	VCC_IN1	PWR_I	5.0V	-	Main Power Supply Input
M25	VCC_IN2	PWR_I	5.0V	-	Main Power Supply Input
N24	VCC_IN3	PWR_I	5.0V	-	Main Power Supply Input
L22	VCC_IN4	PWR_I	5.0V	-	Main Power Supply Input
N22	VCC_IN5	PWR_I	5.0V	-	Main Power Supply Input
M21	VCC_IN6	PWR_I	5.0V	-	Main Power Supply Input
N20	VCC_IN7	PWR_I	5.0V	-	Main Power Supply Input
P21	VCC_IN8	PWR_I	5.0V	-	Main Power Supply Input
AA22	VCC_RTC	PWR_I	3.0V	-	RTC Input Voltage
AA20	VCC_1V8_OUT1	PWR_O	1.8V	-	1.8V Voltage Output
AB21	VCC_1V8_OUT2	PWR_O	1.8V	-	1.8V Voltage Output
AA24	VCC_3V3_OUT1	PWR_O	3.3V	-	3.3V Voltage Output
AB25	VCC_3V3_OUT2	PWR_O	3.3V	-	3.3V Voltage Output

PRELIMINARY

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
AC20	JTAG_TCK	IN	1.8V	AB32	JTAG Test Clock
AC22	JTAG_TDI	IN	1.8V	AC31	JTAG Test Data Input
AD25	JTAG_TDO	OUT	1.8V	AB30	JTAG Test Data Output
AC24	JTAG_TMS	IN	1.8V	AA33	JTAG Test Mode Select
AE24	JTAG_TRST	IN	1.8V	AC33	JTAG Reset
U22	nPWRREADY_OUT	OD_OUT	<=12V	-	Power Ready Out (Active low signal, requires external pullup)
Y21	nRESET_IN	OD_IN	1.8V to VCC_IN	-	Reset In (Active low signal, 10K pullup on SOM)
R22	nRESET_OUT	OD_OUT	1.8V	AF36	Reset Out (Active low signal, 10K pullup on SOM)
U20	RTC_CLKOUT	OUT	1.8V	-	RTC Clock Output
T21	RTC_nINT	OD_OUT	1.8V	-	RTC Interrupt Output (Active low signal)
R20	-	-	-	-	No Connect
P25	BOOT_MODE1	IN	1.8V	AL15	Boot Mode Control Pin 1
R24	BOOT_MODE2	IN	1.8V	AM14	Boot Mode Control Pin 2
T25	BOOT_MODE3	IN	1.8V	AM12	Boot Mode Control Pin 3
U24	BOOT_MODE4	IN	1.8V	AG17	Boot Mode Control Pin 4
V57	SDCARD_nCD	OD_IN	1.8V	AG37	SD Card Card Detect
W60	SDCARD_CLK	OUT	1.8V/2.96V	AJ35	SD Card Clock
W58	SDCARD_CMD	I/O	1.8V/2.96V	AH36	SD Card Command (49.9K pullup on SOM)
W62	SDCARD_DATA0	I/O	1.8V/2.96V	AL33	SD Card Data 0 (49.9K pullup on SOM)
Y61	SDCARD_DATA1	I/O	1.8V/2.96V	AK34	SD Card Data 1 (49.9K pullup on SOM)
U60	SDCARD_DATA2	I/O	1.8V/2.96V	AK36	SD Card Data 2 (49.9K pullup on SOM)
V61	SDCARD_DATA3	I/O	1.8V/2.96V	AL35	SD Card Data 3 (49.9K pullup on SOM)
Y57	SDCARD_VCC_OUT	PWR_O	2.96V	-	SD Card Power Supply
V67	SDCARD_nWP	OD_IN	1.8V	AJ31	SD Card Write Protect
AC60	-	-	-	-	No Connect
AD61	USB1_D_N	I/O	Differential	K30	USB1 2.0 Data Negative
AC62	USB1_D_P	I/O	Differential	K32	USB1 2.0 Data Positive
AE60	USB1_ID	IN	1.8V	AH18	USB1 ID
AE58	USB1_nOC	IN	1.8V	AM10	USB1 Over Current (Active low signal)
AD57	USB1_PWR_EN	OUT	1.8V	AJ23	USB1 Power Enable
AF67	USB1_RX0_N	IN	Differential	K36	USB1 3.0 Receive Negative
AE66	USB1_RX0_P	IN	Differential	K34	USB1 3.0 Receive Positive
AF71	USB1_TX0_N	OUT	Differential	R37	USB1 3.0 Transmit Negative
AE70	USB1_TX0_P	OUT	Differential	R35	USB1 3.0 Transmit Positive
AA58	-	-	-	-	No Connect
AB61	USB2_D_N	I/O	Differential	M30	USB2 2.0 Data Negative
AA62	USB2_D_P	I/O	Differential	M32	USB2 2.0 Data Positive
AA60	USB2_ID	IN	1.8V	AM22	USB2 ID
AC58	USB2_nOC	IN	1.8V	AL21	USB2 Over Current (Active low signal)
AB57	USB2_PWR_EN	OUT	1.8V	AJ21	USB2 Power Enable
AC66	-	-	-	-	No Connect
AB67	-	-	-	-	No Connect
AC70	-	-	-	-	No Connect
AB71	-	-	-	-	No Connect
AH57	GB_ETH1_A_N	I/O	Differential	-	Ethernet Data A Negative
AJ58	GB_ETH1_A_P	I/O	Differential	-	Ethernet Data A Positive
AF57	GB_ETH1_B_N	I/O	Differential	-	Ethernet Data B Negative
AG58	GB_ETH1_B_P	I/O	Differential	-	Ethernet Data B Positive
AG62	GB_ETH1_C_N	I/O	Differential	-	Ethernet Data C Negative

PRELIMINARY

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
AH61	GB_ETH1_C_P	I/O	Differential	-	Ethernet Data C Positive
AE62	GB_ETH1_D_N	I/O	Differential	-	Ethernet Data D Negative
AF61	GB_ETH1_D_P	I/O	Differential	-	Ethernet Data D Positive
AG60	GB_ETH1_LED_ACT	OD_OUT	<= 5V	-	Ethernet LED Activity Signal
AJ60	GB_ETH1_LED_LINK	OD_OUT	<= 5V	-	Ethernet LED Link Signal
AH45	RGMII2_EVENT_IN	IN	1.8V	AK18	RGMII2 Event In
AJ44	RGMII2_EVENT_OUT	OUT	1.8V	AK16	RGMII2 Event Out
AG46	RGMII2_MDC	OUT	1.8V	V10	RGMII2 Management Data Clock
AG44	RGMII2_MDIO	I/O	1.8V	W11	RGMII2 Management Data IO
AG48	RGMII2_nINT	IN	1.8V	R9	RGMII2 Interrupt
AG54	RGMII2_RX_CTL	IN	1.8V	T6	RGMII2 Receive Control
AJ56	RGMII2_RX_D0	IN	1.8V	T8	RGMII1 Receive Data 0
AJ54	RGMII2_RX_D1	IN	1.8V	T10	RGMII1 Receive Data 1
AJ52	RGMII2_RX_D2	IN	1.8V	U7	RGMII1 Receive Data 2
AH53	RGMII2_RX_D3	IN	1.8V	U9	RGMII1 Receive Data 3
AG56	RGMII2_RXC	IN	1.8V	U11	RGMII1 Receive Clock
AG50	RGMII2_TX_CTL	OUT	1.8V	Y10	RGMII2 Transmit Control
AJ50	RGMII2_TX_D0	OUT	1.8V	Y8	RGMII1 Transmit Data 0
AJ48	RGMII2_TX_D1	OUT	1.8V	Y6	RGMII1 Transmit Data 1
AH49	RGMII2_TX_D2	OUT	1.8V	W7	RGMII1 Transmit Data 2
AJ46	RGMII2_TX_D3	OUT	1.8V	W9	RGMII1 Transmit Data 3
AG52	RGMII2_TXC	OUT	1.8V	V6	RGMII1 Transmit Clock
R62	CSI1_CLK_N	IN	Differential	K6	CSI1 Clock Negative
R60	CSI1_CLK_P	IN	Differential	J7	CSI1 Clock Positive
T57	CSI1_D0_N	IN	Differential	L5	CSI1 Data 0 Negative
U58	CSI1_D0_P	IN	Differential	K4	CSI1 Data 0 Positive
T61	CSI1_D1_N	IN	Differential	L7	CSI1 Data 1 Negative
U62	CSI1_D1_P	IN	Differential	K8	CSI1 Data 1 Positive
P57	CSI1_D2_N	IN	Differential	M10	CSI1 Data 2 Negative
R58	CSI1_D2_P	IN	Differential	L9	CSI1 Data 2 Positive
N62	CSI1_D3_N	IN	Differential	M8	CSI1 Data 3 Negative
P61	CSI1_D3_P	IN	Differential	M6	CSI1 Data 3 Positive
H41	CSI2_CLK_N	IN	Differential	K2	CSI2 Clock Negative
J42	CSI2_CLK_P	IN	Differential	J1	CSI2 Clock Positive
G42	CSI2_D0_N	IN	Differential	L1	CSI2 Data 0 Negative
G44	CSI2_D0_P	IN	Differential	L3	CSI2 Data 0 Positive
J44	CSI2_D1_N	IN	Differential	M4	CSI2 Data 1 Negative
H45	CSI2_D1_P	IN	Differential	M2	CSI2 Data 1 Positive
J38	CSI2_D2_N	IN	Differential	N3	CSI2 Data 2 Negative
J40	CSI2_D2_P	IN	Differential	N1	CSI2 Data 2 Positive
G38	CSI2_D3_N	IN	Differential	P4	CSI2 Data 3 Negative
G40	CSI2_D3_P	IN	Differential	P2	CSI2 Data 3 Positive
AN46	DSI1_CLK_N	OUT	Differential	R29	DSI1 Clock Negative
AN48	DSI1_CLK_P	OUT	Differential	P30	DSI1 Clock Positive
AL48	DSI1_D0_N	OUT	Differential	U33	DSI1 Data 0 Negative
AL50	DSI1_D0_P	OUT	Differential	V32	DSI1 Data 0 Positive
AM49	DSI1_D1_N	OUT	Differential	T32	DSI1 Data 1 Negative
AN50	DSI1_D1_P	OUT	Differential	R33	DSI1 Data 1 Positive
AN44	DSI1_D2_N	OUT	Differential	V30	DSI1 Data 2 Negative
AM45	DSI1_D2_P	OUT	Differential	U29	DSI1 Data 2 Positive
AL44	DSI1_D3_N	OUT	Differential	T30	DSI1 Data 3 Negative
AL46	DSI1_D3_P	OUT	Differential	U31	DSI1 Data 3 Positive

PRELIMINARY

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
N52	LVDS1_CLK_N	OUT	Differential	-	LVDS1 Clock Negative
N50	LVDS1_CLK_P	OUT	Differential	-	LVDS1 Clock Positive
L52	LVDS1_DATA0_N	OUT	Differential	-	LVDS1 Data 0 Negative
L50	LVDS1_DATA0_P	OUT	Differential	-	LVDS1 Data 0 Positive
L54	LVDS1_DATA1_N	OUT	Differential	-	LVDS1 Data 1 Negative
M53	LVDS1_DATA1_P	OUT	Differential	-	LVDS1 Data 1 Positive
N56	LVDS1_DATA2_N	OUT	Differential	-	LVDS1 Data 2 Negative
N54	LVDS1_DATA2_P	OUT	Differential	-	LVDS1 Data 2 Positive
M57	LVDS1_DATA3_N	OUT	Differential	-	LVDS1 Data 3 Negative
L56	LVDS1_DATA3_P	OUT	Differential	-	LVDS1 Data 3 Positive
N40	GPIO1	I/O	1.8V	G3	GPIO Pin 1
L40	GPIO2	I/O	1.8V	G1	GPIO Pin 2
AL32	GPIO3	I/O	1.8V	E3	GPIO Pin 3
AL34	GPIO4	I/O	1.8V	AM20	GPIO Pin 4
AN30	GPIO5	I/O	1.8V	Y36	GPIO Pin 5
AN32	GPIO6	I/O	1.8V	E1	GPIO Pin 6
AN34	GPIO7	I/O	1.8V	G5	GPIO Pin 7
N48	PWM1	OUT	1.8V	H4	General PWM 1
N58	PWM2	OUT	1.8V	D2	General PWM 2
AL42	PWM3	OUT	1.8V	AK22	General PWM 3
AN52	PWM4	OUT	1.8V	AK14	General PWM 4
L26	I2C1_SCL_DNU	OD_IO	1.8V	AL27	I2C1 Clock (Not recommended for use due to internal usage, 2.2K pullup on SOM)
L28	I2C1_SDA_DNU	OD_IO	1.8V	AK26	I2C1 Data (Not recommended for use due to internal usage, 2.2K pullup on SOM)
L60	I2C2_SCL	OD_IO	1.8V	G9	I2C2 Clock
L58	I2C2_SDA	OD_IO	1.8V	G7	I2C2 Data
M61	I2C3_SCL	OD_IO	1.8V	AL23	I2C3 Clock
N60	I2C3_SDA	OD_IO	1.8V	AM24	I2C3 Data
AN36	I2C4_SCL	OD_IO	1.8V	F4	I2C4 Clock
AN38	I2C4_SDA	OD_IO	1.8V	F2	I2C4 Data
AN40	I2C5_SCL	OD_IO	1.8V	AK28	I2C5 Clock
AN42	I2C5_SDA	OD_IO	1.8V	AM28	I2C5 Data
AJ32	SAI1_MCLK	OUT	1.8V	AK32	SAI1 Master Clock
AG32	-	-	-	-	No Connect
AG28	-	-	-	-	No Connect
AG30	SAI1_RX_DATA	IN	1.8V	AF32	SAI1 Receive Data
AJ30	SAI1_TX_SYNC	OUT	1.8V	AD34	SAI1 Transmit Frame Sync
AH29	SAI1_TX_BCLK	OUT	1.8V	AE33	SAI1 Transmit Bit Clock
AJ28	SAI1_TX_DATA	OUT	1.8V	AF34	SAI1 Transmit Data
L34	SPI1_nCS	OUT	1.8V	AJ29	SPI1 Chip Select
N34	SPI1_MISO	IN	1.8V	AK30	SPI1 Master in, Slave out
N32	SPI1_MOSI	OUT	1.8V	AL29	SPI1 Master out, Slave in
M33	SPI1_SCLK	OUT	1.8V	AH28	SPI1 Clock
N30	SPI2_nCS	OUT	1.8V	AJ27	SPI2 Chip Select
L32	SPI2_MISO	IN	1.8V	AF26	SPI2 Master in, Slave out
L30	SPI2_MOSI	OUT	1.8V	AG27	SPI2 Master out, Slave in
M29	SPI2_SCLK	OUT	1.8V	AH26	SPI2 Clock
AM41	SPI3_nCS	OUT	1.8V	AA7	SPI3 Chip Select
AL36	SPI3_MISO	IN	1.8V	AB8	SPI3 Master in, Slave out
AL38	SPI3_MOSI	OUT	1.8V	AB10	SPI3 Master out, Slave in
AL40	SPI3_SCLK	OUT	1.8V	AA9	SPI3 Clock
M41	UART1_CTS	IN	1.8V	AE15	UART1 Clear to Send

PRELIMINARY

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
N42	UART1_RTS	OUT	1.8V	AH16	UART1 Request to Send
L44	UART1_RXD	IN	1.8V	AF16	UART1 Receive
L42	UART1_TXD	OUT	1.8V	AG15	UART1 Transmit
L46	UART2_CTS	IN	1.8V	AH30	UART2 Clear to Send
M45	UART2_RTS	OUT	1.8V	AG29	UART2 Request to Send
N46	UART2_RXD	IN	1.8V	AJ25	UART2 Receive
N44	UART2_TXD	OUT	1.8V	AG25	UART2 Transmit
AE22	UART3_RXD	IN	1.8V	AM26	UART3 Receive
AE20	UART3_TXD	OUT	1.8V	AL25	UART3 Transmit
AJ24	QSPI_nCE	OUT	1.8V	AD28	QSPI Chip Enable (Active low signal)
AG24	QSPI_CLK	OUT	1.8V	AF28	QSPI Clock
AF21	QSPI_DATA_0	I/O	1.8V	AE29	QSPI Data 0
AG20	QSPI_DATA_1	I/O	1.8V	AM30	QSPI Data 1
AG22	-	-	-	-	No Connect
AH21	-	-	-	-	No Connect
AJ22	-	-	-	-	No Connect
AA14	PCIE1_CLK_N	OUT	Differential	U1	PCIe1 Reference Clock Negative
AB15	PCIE1_CLK_P	OUT	Differential	U3	PCIe1 Reference Clock Positive
AC16	PCIE1_nCLKREQ	IN	1.8V	P6	PCIe1 Clock Request
AC14	PCIE1_nPERST	OUT	1.8V	P8	PCIe1 Reset
AB11	PCIE1_RXN_N	IN	Differential	Y2	PCIe1 Receive Data Negative
AC12	PCIE1_RXN_P	IN	Differential	Y4	PCIe1 Receive Data Positive
Y11	PCIE1_TXN_N	OUT	Differential	T4	PCIe1 Transmit Data Negative
AA12	PCIE1_TXN_P	OUT	Differential	T2	PCIe1 Transmit Data Positive
M23	GND	-	-	-	Ground
P23	GND	-	-	-	Ground
T23	GND	-	-	-	Ground
V23	GND	-	-	-	Ground
Y23	GND	-	-	-	Ground
V59	GND	-	-	-	Ground
T59	GND	-	-	-	Ground
P59	GND	-	-	-	Ground
M59	GND	-	-	-	Ground
M55	GND	-	-	-	Ground
M51	GND	-	-	-	Ground
M47	GND	-	-	-	Ground
M43	GND	-	-	-	Ground
M39	GND	-	-	-	Ground
M35	GND	-	-	-	Ground
M31	GND	-	-	-	Ground
M27	GND	-	-	-	Ground
M13	GND	-	-	-	Ground
P13	GND	-	-	-	Ground
T13	GND	-	-	-	Ground
V13	GND	-	-	-	Ground
Y13	GND	-	-	-	Ground
V69	GND	-	-	-	Ground
T69	GND	-	-	-	Ground
P69	GND	-	-	-	Ground
M69	GND	-	-	-	Ground
H59	GND	-	-	-	Ground
H55	GND	-	-	-	Ground

PRELIMINARY

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
H51	GND	-	-	-	Ground
H47	GND	-	-	-	Ground
H43	GND	-	-	-	Ground
H39	GND	-	-	-	Ground
H35	GND	-	-	-	Ground
H31	GND	-	-	-	Ground
H27	GND	-	-	-	Ground
H23	GND	-	-	-	Ground
AB23	GND	-	-	-	Ground
AD23	GND	-	-	-	Ground
AF23	GND	-	-	-	Ground
AH23	GND	-	-	-	Ground
AH27	GND	-	-	-	Ground
AH31	GND	-	-	-	Ground
AH35	GND	-	-	-	Ground
AH39	GND	-	-	-	Ground
AH43	GND	-	-	-	Ground
AH47	GND	-	-	-	Ground
AH51	GND	-	-	-	Ground
AH55	GND	-	-	-	Ground
AH59	GND	-	-	-	Ground
AF59	GND	-	-	-	Ground
AD59	GND	-	-	-	Ground
AB59	GND	-	-	-	Ground
Y59	GND	-	-	-	Ground
AB13	GND	-	-	-	Ground
AD13	GND	-	-	-	Ground
AF13	GND	-	-	-	Ground
AH13	GND	-	-	-	Ground
AM23	GND	-	-	-	Ground
AM27	GND	-	-	-	Ground
AM31	GND	-	-	-	Ground
AM35	GND	-	-	-	Ground
AM39	GND	-	-	-	Ground
AM43	GND	-	-	-	Ground
AM47	GND	-	-	-	Ground
AM51	GND	-	-	-	Ground
AM55	GND	-	-	-	Ground
AM59	GND	-	-	-	Ground
AH69	GND	-	-	-	Ground
AF69	GND	-	-	-	Ground
AD69	GND	-	-	-	Ground
AB69	GND	-	-	-	Ground
Y69	GND	-	-	-	Ground
C26	GND	-	-	-	Ground
C30	GND	-	-	-	Ground
C34	GND	-	-	-	Ground
C38	GND	-	-	-	Ground
C44	GND	-	-	-	Ground
C48	GND	-	-	-	Ground
C52	GND	-	-	-	Ground
C56	GND	-	-	-	Ground

PRELIMINARY

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
E30	GND	-	-	-	Ground
E36	GND	-	-	-	Ground
E46	GND	-	-	-	Ground
E52	GND	-	-	-	Ground
K7	GND	-	-	-	Ground
K75	GND	-	-	-	Ground
N8	GND	-	-	-	Ground
N74	GND	-	-	-	Ground
T7	GND	-	-	-	Ground
T75	GND	-	-	-	Ground
W8	GND	-	-	-	Ground
W74	GND	-	-	-	Ground
AA8	GND	-	-	-	Ground
AA74	GND	-	-	-	Ground
AD7	GND	-	-	-	Ground
AD75	GND	-	-	-	Ground
AG8	GND	-	-	-	Ground
AG74	GND	-	-	-	Ground
AK7	GND	-	-	-	Ground
AK75	GND	-	-	-	Ground
AR30	GND	-	-	-	Ground
AR36	GND	-	-	-	Ground
AR46	GND	-	-	-	Ground
AR52	GND	-	-	-	Ground
AU26	GND	-	-	-	Ground
AU30	GND	-	-	-	Ground
AU34	GND	-	-	-	Ground
AU38	GND	-	-	-	Ground
AU44	GND	-	-	-	Ground
AU48	GND	-	-	-	Ground
AU52	GND	-	-	-	Ground
AU56	GND	-	-	-	Ground
AM21	-	-	-	-	No Connect
AM25	-	-	-	-	No Connect
AL24	-	-	-	-	No Connect
AL26	-	-	-	-	No Connect
AN26	-	-	-	-	No Connect
AN28	-	-	-	-	No Connect
AN22	-	-	-	-	No Connect
AN24	-	-	-	-	No Connect
AM61	-	-	-	-	No Connect
AN60	-	-	-	-	No Connect
AL58	-	-	-	-	No Connect
AL56	-	-	-	-	No Connect
AN58	-	-	-	-	No Connect
AM57	-	-	-	-	No Connect
AL54	-	-	-	-	No Connect
AL52	-	-	-	-	No Connect
AN56	-	-	-	-	No Connect
AN54	-	-	-	-	No Connect
AG16	-	-	-	-	No Connect
AF15	-	-	-	-	No Connect

PRELIMINARY

X1, Mandatory/Optional Pins					
Pin	**FPSC Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
AG12	-	-	-	-	No Connect
AF11	-	-	-	-	No Connect
AE16	-	-	-	-	No Connect
AD15	-	-	-	-	No Connect
AE12	-	-	-	-	No Connect
AD11	-	-	-	-	No Connect
AH11	-	-	-	-	No Connect
AE14	-	-	-	-	No Connect
AG14	-	-	-	-	No Connect
AJ12	-	-	-	-	No Connect
AJ14	-	-	-	-	No Connect
AH15	-	-	-	-	No Connect
N36	-	-	-	-	No Connect
N38	-	-	-	-	No Connect
M37	-	-	-	-	No Connect
L38	-	-	-	-	No Connect
H21	-	-	-	-	No Connect
G20	-	-	-	-	No Connect
R16	-	-	-	-	No Connect
T15	-	-	-	-	No Connect
U16	-	-	-	-	No Connect
U14	-	-	-	-	No Connect
V15	-	-	-	-	No Connect
W16	-	-	-	-	No Connect
W14	-	-	-	-	No Connect
Y15	-	-	-	-	No Connect
J56	-	-	-	-	No Connect
G54	-	-	-	-	No Connect
J58	-	-	-	-	No Connect
H57	-	-	-	-	No Connect
G56	-	-	-	-	No Connect
G62	-	-	-	-	No Connect
H61	-	-	-	-	No Connect
G60	-	-	-	-	No Connect
G58	-	-	-	-	No Connect

Table 3 phyFLEX-AM62Px Connector X1, Specialized Pinout

X1, Column B					
Pin	**Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
G22	VDD_3V3	PWR	3.3V	-	3.3V Primary Power
G24	VDD_3V3	PWR	3.3V	-	3.3V Primary Power
G26	VDD_3V3	PWR	3.3V	-	3.3V Primary Power
G28	VDD_3V3	PWR	3.3V	-	3.3V Primary Power
G30	VDD_3V3	PWR	3.3V	-	3.3V Primary Power
G32	X_GPIO_86	I/O	1.8V	Y34	GPIO
G34	X_GPIO_87	I/O	1.8V	AA35	GPIO
G36	X_GPIO_88	I/O	1.8V	AH2	GPIO
G46	X_GPIO_152	I/O	1.8V	H28	GPIO
G48	VDD_L6A_0V928	PWR_O	0.928V	-	Do not use, intended for debug purposes only
G50	VDD_L7A	PWR_O	-	-	Do not use, intended for debug purposes only

PRELIMINARY

X1, Column B					
Pin	**Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
G52	VDD_L8A_1V304	PWR_O	1.304V	-	Do not use, intended for debug purposes only
H25	X_GPIO_102	I/O	1.8V	AE31	GPIO
H29	X_GPIO_103	I/O	1.8V	AG33	GPIO
H33	X_GPIO_104	I/O	1.8V	AH32	GPIO
H37	X_GPIO_105	I/O	1.8V	AJ33	GPIO
H49	VDD_L9A_0V928	PWR_O	0.928V	-	Do not use, intended for debug purposes only
H53	VDD_L10A_2V96	PWR_O	2.96V	-	Do not use, intended for debug purposes only
J24	VDD_L11A_1V248	PWR_O	1.248V	-	Do not use, intended for debug purposes only
J26	X_GPIO30	I/O	1.8V	AH24	GPIO
J28	X_GPIO31	I/O	1.8V	AF24	GPIO
J30	X_GPIO_76	I/O	1.8V	AA37	GPIO
J32	X_GPIO_114	I/O	1.8V	AB36	GPIO
J34	X_GPIO_115	I/O	1.8V	AG3	GPIO
J36	X_GPIO_116	I/O	1.8V	AH4	GPIO
J46	VDD_L12A_1V8	PWR_O	1.8V	-	Do not use, intended for debug purposes only
J48	VDD_L13A_3V128	PWR_O	3.128V	-	Do not use, intended for debug purposes only
J50	X_PHY_EEPROM_WCn	I	1.8V	-	EEPROM Write Protect (10K pullup on SOM)
J52	VDD_L14A	PWR_O	-	-	Do not use, intended for debug purposes only
J54	X_RTC_EVI	I	1.8V	-	RTC Event Input (10K pullup on SOM)
L12	X_GPIO_79	I/O	1.8V	AK20	GPIO
L14	X_GPIO_77	I/O	1.8V	AL19	GPIO
L36	X_GPIO_153	I/O	1.8V	G29	GPIO
L48	X_GPIO_154	I/O	1.8V	F30	GPIO
L68	VDD_L15A_1V8	PWR_O	1.8V	-	Do not use, intended for debug purposes only
L70	VDD_L16A_2V5	PWR_O	2.5V	-	Do not use, intended for debug purposes only
M11	X_GPIO_66/BT_CFG_4[1]	I/O	1.8V	AJ19	GPIO/Boot Config
M15	X_GPIO_68/BT_CFG_5[1]	I/O	1.8V	AM18	GPIO/Boot Config
M49	X_GPIO_70/BT_CFG_6[1]	I/O	1.8V	AE17	GPIO/Boot Config
M67	X_GPIO_72/BT_CFG_7[1]	I/O	1.8V	AF18	GPIO/Boot Config
M71	X_GPIO_54/BT_CFG_8[1]	I/O	1.8V	AJ17	GPIO/Boot Config
N12	X_GPIO_55/BT_CFG_9[1]	I/O	1.8V	AJ15	GPIO/Boot Config
N14	X_GPIO_56/BT_CFG_10[1]	I/O	1.8V	AL17	GPIO/Boot Config
N16	X_GPIO_57/BT_CFG_11[1]	I/O	1.8V	AM16	GPIO/Boot Config
N28	X_GPIO_151/RGMII1_RESETn	I/O	1.8V	V8	RGMII1 Reset
N66	X_JTAG_SRST_N	IN	1.8V	AC29	JTAG reset for debug
N68	X_GPIO_91	I/O	1.8V	H32	GPIO
N70	X_GPIO_92	I/O	1.8V	G31	GPIO
P11	X_GPIO_93/FORCE_USB_BOOT[1]	I/O	1.8V	G33	Force USB Boot
P15	X_GPIO_94	I/O	1.8V	AG35	GPIO
P67	X_GPIO_95	I/O	1.8V	AD30	GPIO
P71	X_GPIO_100	I/O	1.8V	AD32	GPIO
R12	X_GPIO_101	I/O	1.8V	AG31	GPIO
R14	X_GPIO_106	I/O	1.8V	AF30	GPIO
R66	X_GPIO_107	I/O	1.8V	AL31	GPIO
R68	X_GPIO_108	I/O	1.8V	AM32	GPIO
R70	X_GPIO_111	I/O	1.8V	AB34	GPIO
T11	X_GPIO_112	I/O	1.8V	AC35	GPIO
T67	X_GPIO_113	I/O	1.8V	AC37	GPIO
T71	X_GPIO_119	I/O	1.8V	R7	GPIO
U12	X_PMIC_CBLPWR_N	IN	1.8V	-	Power on Trigger for PMIC
U66	X_DSI0_CLK1_M	OUT	Differential	R31	DSI0 Clock 1 Negative
U68	X_DSI0_CLK1_P	OUT	Differential	P32	DSI0 Clock 1 Positive
U70	VDD_L1A	PWR_O	-	-	Do not use, intended for debug purposes only

PRELIMINARY

X1, Column B					
Pin	**Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
V11	X_PMIC_RF_CLK2	OUT	1.2V	-	PMIC Reference Clock 2
V21	X_PMIC_RESIN_N	IN	1.8V	-	Reset input to PMIC
V25	X_PMIC_SYSTEM_ON	IN	1.8V	-	PMIC power on trigger
V71	VDD_L2A_2V96	PWR_O	2.96V	-	Do not use, intended for debug purposes only
W12	X_PMIC_GPIO02	I/O	1.8V	-	GPIO
W20	X_PMIC_FAULT_N	I/O	1.8V	-	PMIC fault signal
W22	X_PMIC_GPIO04	I/O	1.8V	-	GPIO
W24	X_PMIC_GPIO05	I/O	1.8V/3.3V	-	GPIO
W66	X_PMIC_GPIO06	I/O	1.8V/3.3V	-	GPIO
W68	X_PMIC_GPIO07	I/O	1.8V/3.3V	-	GPIO
W70	X_GPIO_26	I/O	1.8V		GPIO
Y25	X_GPIO_27	I/O	1.8V		GPIO
Y67	X_PMIC_GPIO10	I/O	1.8V/3.3V	-	GPIO
Y71	X_PMIC_GPIO01	I/O	1.8V	-	GPIO
AA16	X_PMIC_GPIO03	I/O	1.8V	-	GPIO
AA66	X_PMIC_RF_CLK3	OUT	1.2V	-	PMIC Reference Clock 3
AA68	X_PMIC_LN_BB_CLK3	OUT	1.8V	-	PMIC Clock 3
AA70	VDD_L3A_1V0	PWR_O	1.0V	-	Do not use, intended for debug purposes only
AC68	X_PMIC_GPIO08	I/O	1.8V/3.3V	-	GPIO
AD21	VDD_L4A_0V928	PWR_O	0.928V	-	Do not use, intended for debug purposes only
AD67	X_MODE_0	IN	1.8V	AE23	Mode control bit 0
AD71	X_MODE_1	IN	1.8V	AG23	Mode control bit 1
AE68	X_PMIC_GPIO09	I/O	1.8V/3.3V	-	GPIO
AF25	VDD_L17A_2V96	PWR_O	2.96V	-	Do not use, intended for debug purposes only
AG26	VDD_L18A_0V664	PWR_O	0.664V	-	Do not use, intended for debug purposes only
AG34	X_WLAN_TX_I_M	OUT	Differential	AH8	WLAN transmit in-phase negative
AG36	X_WLAN_TX_Q_M	OUT	Differential	AJ7	WLAN transmit quadrature negative
AG38	X_WLAN_BBD_CLK	OUT	-	AL3	WLAN baseband command clock
AG40	X_WLAN_BBD_DATA	I/O	-	AK4	WLAN baseband command data
AG42	VDD_L5A_0V928	PWR_O	0.928V	-	Do not use, intended for debug purposes only
AG66	X_USB0_SS_RX1_P	IN	Differential	H36	USB0 super speed receive 1 positive
AG68	NC	-	-	-	No Connect
AG70	X_USB0_SS_TX1_P	OUT	Differential	N35	USB0 super speed transmit 1 positive
AH25	X_WLAN_CXM_CLK	OUT	-	AM6	WLAN coexistence module command clock
AH33	X_WLAN_CXM_DATA	I/O	-	AL5	WLAN coexistence module command data
AH37	X_WLAN_RX_I_P	IN	Differential	AF10	WLAN receive in-phase positive
AH41	X_WLAN_RX_Q_P	IN	Differential	AF12	WLAN receive quadrature negative
AH67	X_USB0_SS_RX1_M	IN	Differential	J35	USB0 super speed receive 1 negative
AH71	X_USB0_SS_TX1_M	OUT	Differential	P36	USB0 super speed transmit 1 neagtive
AJ26	X_WLAN_TX_I_P	OUT	Differential	AG7	WLAN transmit in-phase positive
AJ34	X_WLAN_TX_Q_P	OUT	Differential	AJ9	WLAN transmit quadrature positive
AJ36	X_WLAN_RX_I_M	IN	Differential	AG11	WLAN receive in-phase negative
AJ38	X_WLAN_RX_Q_M	IN	Differential	AH12	WLAN receive quadrature negative
AJ40	X_GNSS_BB_I	IN	-	AG21	GNSS baseband in-phase (I-path) input
AJ42	X_GNSS_BB_Q	IN	-	AF20	GNSS baseband quadrature (Q-path) input
AJ68	VDD_S1A_S10A_0V872	PWR_O	0.872V	-	Do not use, intended for debug purposes only
AJ70	VDD_S2A_S3A_0V8	PWR_O	0.8V	-	Do not use, intended for debug purposes only
AL28	VDD_S4A_1V8	PWR_O	1.8V	-	Do not use, intended for debug purposes only
AL30	VDD_S5A_1V872	PWR_O	1.872V	-	Do not use, intended for debug purposes only
AM29	VDD_S6A_1V348	PWR_O	1.348V	-	Do not use, intended for debug purposes only
AM33	VDD_S7A_1V128	PWR_O	1.128V	-	Do not use, intended for debug purposes only
AM37	VDD_S8A_0V616	PWR_O	0.616V	-	Do not use, intended for debug purposes only
AM53	VDD_S9A_0V88	PWR_O	0.88V	-	Do not use, intended for debug purposes only

PRELIMINARY

X1, Column B					
Pin	**Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
AN20	NC	-	-	-	No Connect
AN62	X_PMIC_RF_CLK1	OUT	1.2V	-	PMIC Reference Clock 1
E26	NC	-	-	-	No Connect
E28	NC	-	-	-	No Connect
E32	NC	-	-	-	No Connect
E34	NC	-	-	-	No Connect
E38	NC	-	-	-	No Connect
E40	NC	-	-	-	No Connect
E42	NC	-	-	-	No Connect
E44	NC	-	-	-	No Connect
E48	NC	-	-	-	No Connect
E50	NC	-	-	-	No Connect
E54	NC	-	-	-	No Connect
E56	NC	-	-	-	No Connect
H7	NC	-	-	-	No Connect
H75	NC	-	-	-	No Connect
J8	NC	-	-	-	No Connect
J74	NC	-	-	-	No Connect
L8	NC	-	-	-	No Connect
L74	NC	-	-	-	No Connect
M7	NC	-	-	-	No Connect
M75	NC	-	-	-	No Connect
P7	NC	-	-	-	No Connect
P75	NC	-	-	-	No Connect
R8	NC	-	-	-	No Connect
R74	NC	-	-	-	No Connect
U8	NC	-	-	-	No Connect
U74	NC	-	-	-	No Connect
V7	NC	-	-	-	No Connect
V75	NC	-	-	-	No Connect
Y7	NC	-	-	-	No Connect
Y75	NC	-	-	-	No Connect
AB7	NC	-	-	-	No Connect
AB75	NC	-	-	-	No Connect
AC8	NC	-	-	-	No Connect
AC74	NC	-	-	-	No Connect
AE8	NC	-	-	-	No Connect
AE74	NC	-	-	-	No Connect
AF7	NC	-	-	-	No Connect
AF75	NC	-	-	-	No Connect
AH7	NC	-	-	-	No Connect
AH75	NC	-	-	-	No Connect
AJ8	NC	-	-	-	No Connect
AJ74	NC	-	-	-	No Connect
AL8	NC	-	-	-	No Connect
AL74	NC	-	-	-	No Connect
AM7	NC	-	-	-	No Connect
AM75	NC	-	-	-	No Connect
AR26	NC	-	-	-	No Connect
AR28	NC	-	-	-	No Connect
AR32	NC	-	-	-	No Connect
AR34	NC	-	-	-	No Connect
AR38	NC	-	-	-	No Connect

PRELIMINARY

X1, Column B					
Pin	**Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
AR40	NC	-	-	-	No Connect
AR42	NC	-	-	-	No Connect
AR44	NC	-	-	-	No Connect
AR48	NC	-	-	-	No Connect
AR50	NC	-	-	-	No Connect
AR54	NC	-	-	-	No Connect
AR56	NC	-	-	-	No Connect

[1:] This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration*.

1.5 Physical Dimensions

TBD

Figure 2. phyFLEX-IQ2390 Dimensions Top View

TBD

Figure 3. phyFLEX-IQ2390 Dimensions Bottom View

TBD

Figure 4. phyFLEX-IQ2390 Dimensions End View

PRELIMINARY

1.6 Technical and Electrical Specifications

Table 4 Technical Specifications

Specification	
Dimensions	48 mm x 45 mm x TBD mm
Mass	TBD
Storage Temperature	-30C to +85C
Operating Temperature	-30C to +85C
Typical Idling Power Consumption[1]	TBD

[1] Calculated from idle I_{vin} in *Table 7*

Table 5 Recommended Operating Conditions for the Input and Output Power Domains

Symbol	Description	Conditions	Min	Typical	Max	Unit
VIN	5V SOM input voltage		4.5	5	5.5	VDC
VBAT	Backup battery for RTC		1.2	3	5.5	VDC
I_{VIN}	5V SOM operating current	Idle in Linux with external interfaces down/disconnected (except for Serial RS-232 and SD card)	-	TBD	-	mA
		Measured while device was under load[1]	-	TBD	-	mA
I_{VBAT}	RTC operating current		-	40	-	nA

[1] The load included the following interfaces/commands: the "memtester 100M" command was run, ETH0 was plugged in with iperf3 running, and four instances of the following command were run (yes > /dev/null &), The Yes Command

Table 6 Additional Resources

Development Tools	
Hardware Manual	TBD
Component Placement	TBD Component Placement Diagram
Symbol/cell	TBD Schematic Symbol and Footprint
Pin Muxing	PHYTEC's pin muxing tool
Schematics	SOM and Carrier Board Schematic References made available upon request here
Free Schematic Review	Contact PHYTEC Support (Schematic reviews completed by PHYTEC Hardware Designer within one week or less)
Software Development	TBD Software documentation

Compliances and Import/Export Data	
RoHS	RoHS II (IPC 1752-A Full Material Declaration available upon request)
REACH	REACH Statement
ECCN	5A992.C
HTS / Schedule B	8471.50.0150

For more information, please contact PHYTEC Sales and Development: http://PHYTEC.com/contact/

PRELIMINARY

2 Revision History

Table 7 Document Revision History

Date	Version Number	Changes in this Manual
2026/08/31	L-1099e.A0	Preliminary Release

PRELIMINARY