

phyCORE-MPC5200B I/O

Hardware Manual

Edition April 2008

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Preface

This phyCORE-MPC5200B-I/O Hardware Manual describes the board's design and functions. Precise specifications for the Freescale MPC5200B microcontroller series can be found in the enclosed MPC5200B microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MPC5200B-I/O



PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MPC5200B-I/O is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and numerous 32-bit controllers on two types of Single Boards Computers:

- (1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
- (2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's target design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MPC5200B-I/O belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC5200B-I/O is a subminiature (53 x 57 mm) insert-ready Single Board Computer populated with Freescale's PowerPC MPC5200B microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the MPC5200B controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC5200B-I/O.

The phyCORE-MPC5200B-I/O offers the following features:

- Single Board Computer in subminiature form factor (84 x 57 mm) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 200-pin Molex connectors
- processor: Freescale embedded PowerPC MPC5200B
- single 3.3 V (max. 1.2 A) supply voltage

Internal Features of the MPC5200B:

- e300 core
 - 760 MIPS at 400 MHz (-40 to +85 °C)
 - 32 k instruction cache, 32 k data cache
 - Double precision FPU
 - Instruction and data MMU
- SDRAM / DDR SDRAM memory Interface
 - up to 132 MHz operation
 - SDRAM and DDR SDRAM support
 - 256 MByte addressing range per CS, two CS available
- Flexible multi-function external bus interface
- Peripheral component interconnect (PCI) controller
- ATA controller
- BestComm DMA subsystem
- 6 programmable serial controllers (PSC), configurable for the following functions:
- Fast Ethernet controller (FEC)
 - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII
- Universal serial bus controller (USB)
 - USB revision 1.1 host
- Two inter-integrated circuit interfaces (I2C)
- Serial peripheral interface (SPI)
- Dual CAN 2.0 A/B controller (MSCAN)
- J1850 byte data link controller (BDLC)
- Test/debug features
- JTAG (IEEE 1149.1 test access port)
- Common on-chip processor (COP) debug port

Memory Configuration¹:

- DDR SDRAM: 64 MByte to 128 MByte
- Flash: up to 64 MByte Intel Strata Flash memory, 32-bit memory width, only asynchronous (J3/P33) devices are supported
- I²C memory: 4 kByte EEPROM

Other Board-Level Features:

- Two UART ports, RS-232 interfaces (RxD/TxD)
- One 10/100 Mbit/s Ethernet port via optional Micrel PHY
- I²C Real-Time Clock with calendar and alarm function
- FPGA with ca. 8000 logic cells, configurable through controller interface or active serial configuration device
- Up to 2 MByte battery buffered SRAM
- Optional industrial temperature range (-40...+85°C)

¹: Please contact PHYTEC for more information about additional module configurations.

1.1 Block Diagram

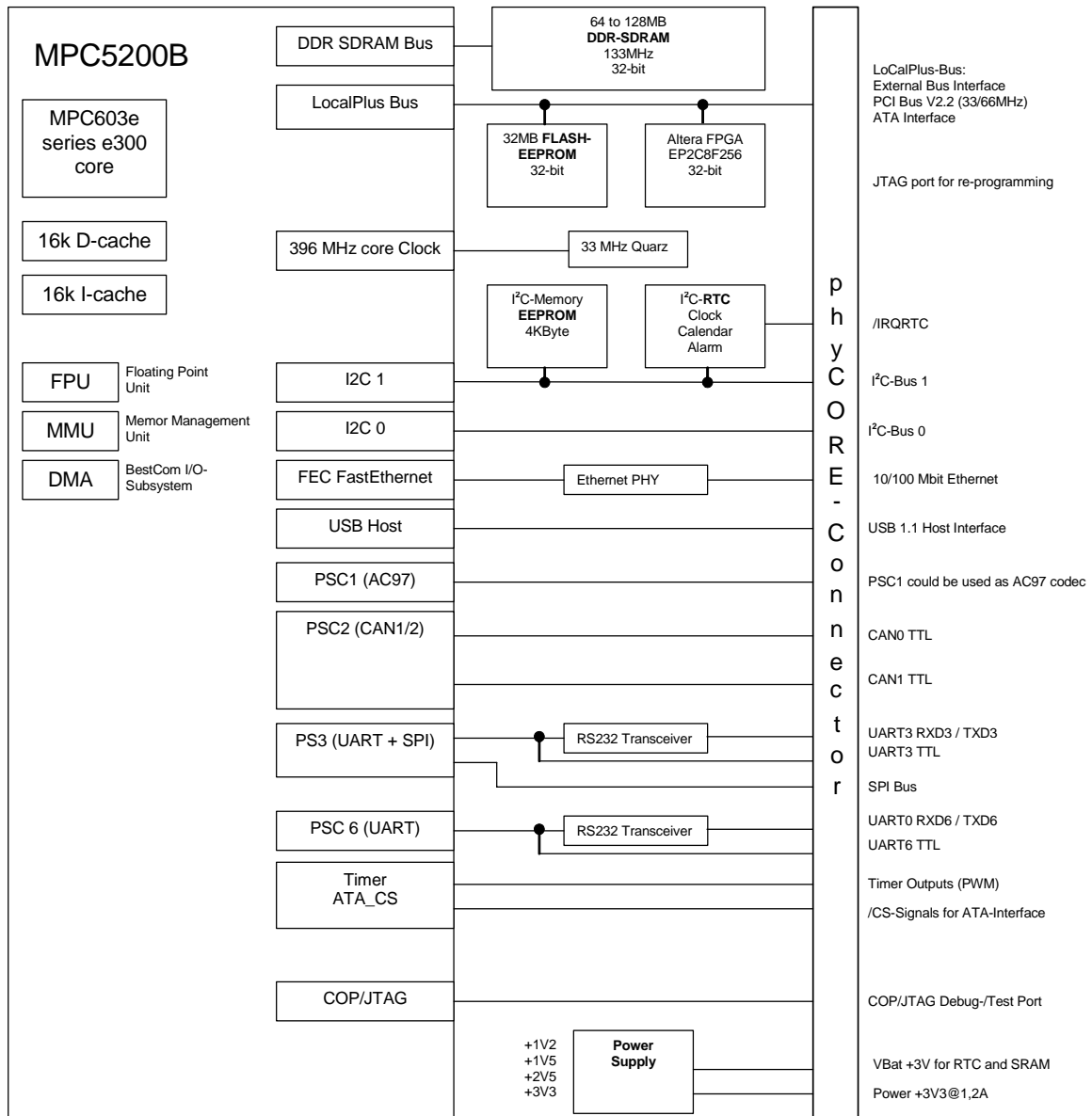


Figure 1: Block Diagram phyCORE-MPC5200B-I/O

1.2 View of the phyCORE-MPC5200B-I/O

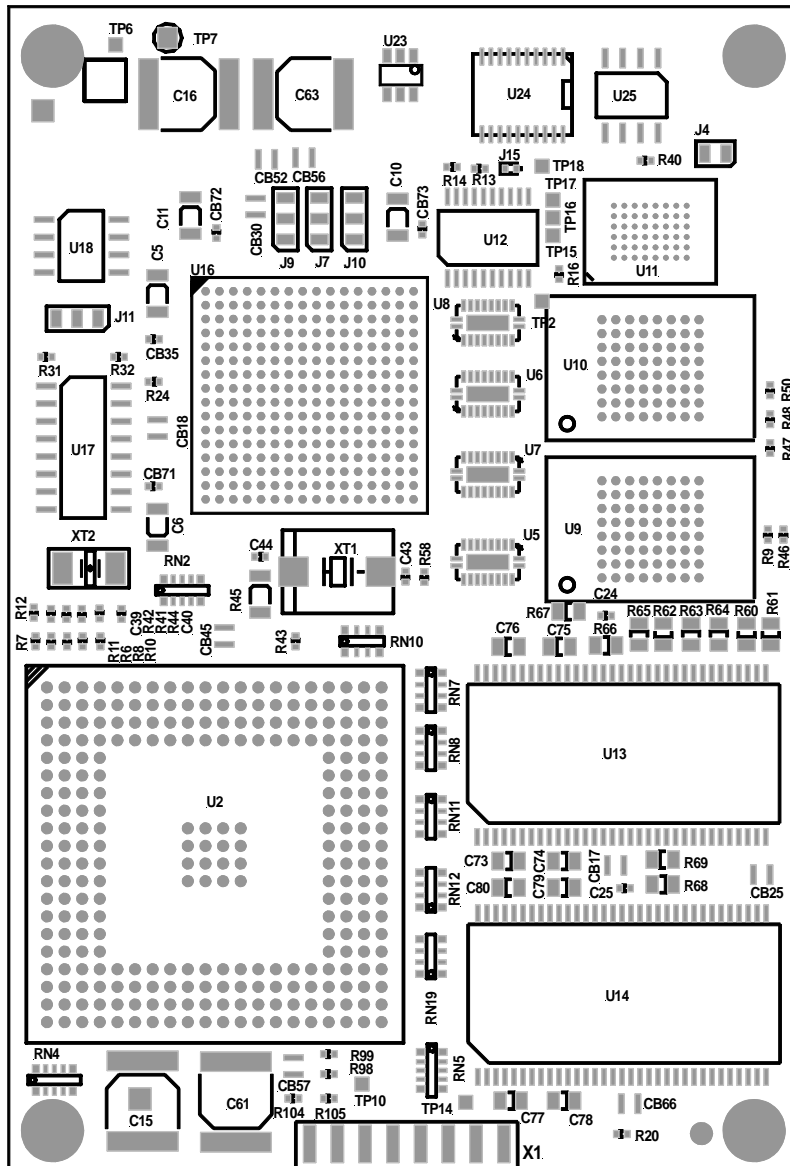


Figure 2: Top View of the phyCORE-MPC5200B-I/O, PCB Rev. 1250.1

1.3 Minimum Requirements to Operate the phyCORE-MPC5200B-I/O

Basic operation of the phyCORE-MPC5200B-I/O only requires supply of a +3V3 input voltage and the corresponding GND connection.

These supply pins are located at the phyCORE-connector X1:

+3V3	X1	1C, 2C, 4C, 5C, 1D, 2D
GND	X1	3C, 3D, 7C, 9D, 12C, 14D

Caution:

We recommend connecting all available +3V3 input pins to the power supply system on a custom carrier board housing the phyCORE-MPC5200B-I/O and at least the matching number of GND pins neighboring the +3V3 pins.

In addition, proper implementation of the phyCORE module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to section 4 for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

Many of the phyCORE-MPC5200B-I/O pins offer alternative functions. These alternative functions must be activated by configuring the applicable controller registers prior to their use. Certain controller functions are pre-configured based on the module's design and are shown in *Table 1*. Signals that are routed directly from the CPU to the Molex connectors can be configured to any available alternative function desired by the user. In contrast, signals that are used on the phyCORE-MPC5200 tiny as listed in *Table 1* can only be used if a special module configuration was purchased (e.g. SBC version without on-board RS-232 transceivers). Please contact PHYTEC for more details.

Note:

The following sections of this manual assume use of the port pins according to configuration listed in *Table 1*.

CPU Port	Function	Port_conf Register Bits	Used on phyCORE SBC
PSC1	AC97_1	01x [29:31]	No
PSC2	CAN 1/2	001 [25:27]	No
PSC3	UART3/SPI	1100 [20:23]	Yes
USB	USB	01 [18:19]	No
Ethernet	Ethernet w/ MD	0101 [12:15]	Yes
Timer	ATA_CS	00_11 [2:3_6:7]	No
I2C	I2C1 / I2C2	default	Yes (I2C1 available)
PSC6	UART6	101 [9:11]	Yes

Table 1: Default Port Configuration

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector; refer to *section 2*). This allows the phyCORE-MPC5200B-I/O to be plugged into any target application like a "big chip".

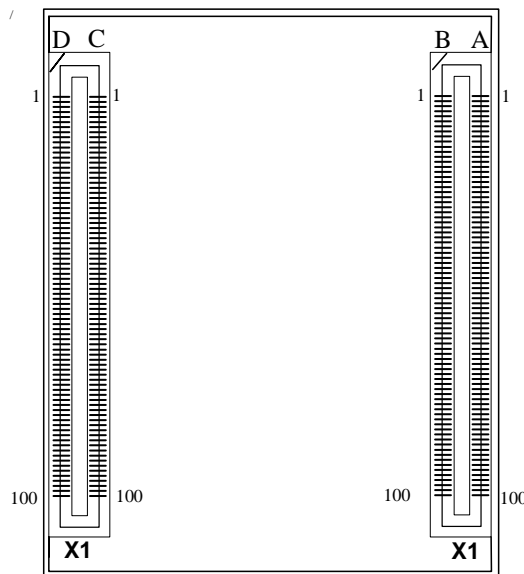


Figure 4: Pinout of the phyCORE-MPC5200B-I/O (Bottom View)

Table 2 provides an overview of the pinout of the phyCORE-connector.

Please refer to the Freescale MPC5200B User Manual/Data Sheet for details on the functions and features of controller signals and port pins.

Pin Number	Signal	I/O	Comments
			FPGA IO Signals
46A	FPGA_B1_J1	I/O	
48A	FPGA_B1_J4	I/O	
49A	FPGA_B1_J6	I/O	
50A	FPGA_B1_K1	I/O	
51A	FPGA_B1_K4	I/O	
53A	FPGA_B1_L2	I/O	
54A	FPGA_B1_L4	I/O	
55A	FPGA_B1_M1	I/O	
56A	FPGA_B1_M3	I/O	
58A	FPGA_B1_N2	I/O	
59A	FPGA_B1_N4	I/O	
60A	FPGA_B1_P1	I/O	
			FPGA JTAG Interface
61A	FPGA_TDO	O	Test Data out
63A	FPGA_TDI	I	Test Data in
		I/O	LocalPlus Address/Data Signals
73A	EXT_AD31		
74A	EXT_AD29		
75A	EXT_AD28		
76A	EXT_AD26		
79A	EXT_AD23		
80A	EXT_AD22		
81A	EXT_AD20		
83A	EXT_AD17		
91A	EXT_AD14		
93A	EXT_AD11		
94A	EXT_AD9		
95A	EXT_AD8		
96A	EXT_AD7		
98A	EXT_AD4		
99A	EXT_AD2		
100A	EXT_AD1		
			ATA Interface Signals
64A	ATA_CS_0	O	Timer Port configured as ATA_CS (Timer0)
65A	ATA_CS_1	O	Timer Port configured as ATA_CS (Timer1)
66A	ATA_IOCHRDY		ATA negated to extend transfer
68A	/ATA_IOR	O	ATA read
69A	ATA_INTRQ	I	ATA interrupt request
			Dedicated PCI Signals
70A	/PCI_RESET	O	Reset output (open drain)
71A	/PCI_GNT	O	Bus grant
78A	/PCI_CBE_3	O	Command byte enable 3
84A	/PCI_CBE_2	O	Command byte enable 2
85A	/PCI_IRDY	O	Initiator (HOST) ready
86A	/PCI_DEVSEL	O	Device select
88A	/PCI_PERR	O	Parity error
89A	/PCI_SERR	O	System Error (open drain)
90A	/PCI_CBE_1	O	Command byte enable 1

Pin Number	Signal	I/O	Comments
Pin Row X1B			
1B	RTC_CLKOUT	O	Clock output of the I ² C RTC U5
2B	/IRQ1	I	Interrupt input 1 of the processor
3B	/IRQ2	I	Interrupt input 2 of the processor
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 41B, 44B, 49B, 54B, 59B, 64B, 69B, 71B, 74B, 79B, 84B, 89B, 94B, 99B	GND		Ground 0 V
5B 6B 7B 33B 35B 36B 47B 48B	/LP_CS3 /LP_CS4 LP_RD/WR /LP_Ts /LP_CS2 /LP_CS5 /LP_CS6 /LP_CS7	O O O O O O O O	LocalPlus Bus Signals Chip Select 3 Chip Select 4 Read not Write Signal (write signal active low) Transfer Start Signal Chip Select 2 Chip Select 5 Chip Select 6 Chip Select 7 (PSC3 is UART3)
8B 10B 11B 12B 13B 15B 16B 17B 18B 20B 21B 22B 23B 25B 26B 27B 28B 30B 31B 32B 37B 38B 40B 41B 42B	FPGA_B2_C11 FPGA_B2_F10 FPGA_B2_F9 FPGA_B2_D11 FPGA_B2_D10 FPGA_B2_B10 FPGA_B2_A10 FPGA_B2_B8 FPGA_B2_A8 FPGA_B2_G7 FPGA_B2_G6 FPGA_B2_E6 FPGA_B2_C5 FPGA_B2_C4 FPGA_B2_A5 FPGA_B2_B5 FPGA_B2_D9 FPGA_B1_C1 FPGA_B1_C2 FPGA_B1_D2 FPGA_B1_D4 FPGA_B1_E2 FPGA_B1_E4 FPGA_B1_E5	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	FPGA IO Signals

Pin Number	Signal	I/O	Comments
			FPGA IO Signals
43B	FPGA_B1_F5	I/O	
45B	FPGA_B1_H6	I/O	
46B	FPGA_B1_J2	I/O	
50B	FPGA_B1_K2	I/O	
51B	FPGA_B1_K5	I/O	
52B	FPGA_B1_L1	I/O	
53B	FPGA_B1_L3	I/O	
55B	FPGA_B1_M2	I/O	
56B	FPGA_B1_M4	I/O	
57B	FPGA_B1_N1	I/O	
58B	FPGA_B1_N3	I/O	
60B	FPGA_B1_P2	I/O	
61B	FPGA_B1_P3	I/O	
			FPGA JTAG Signals
62B	FPGA_TMS	I	Test Mode Select
63B	FPGA_TCK	I	Test Clock
			LocalPlus Address/Data Signals
73B	EXT_AD30	I/O	
75B	EXT_AD27	I/O	
76B	EXT_AD25	I/O	
77B	EXT_AD24	I/O	
80B	EXT_AD21	I/O	
81B	EXT_AD19	I/O	
82B	EXT_AD18	I/O	
83B	EXT_AD16	I/O	
90B	EXT_AD15	I/O	
91B	EXT_AD13	I/O	
92B	EXT_AD12	I/O	
93B	EXT_AD10	I/O	
96B	EXT_AD6	I/O	
97B	EXT_AD5	I/O	
98B	EXT_AD3	I/O	
100B	EXT_AD0	I/O	
			ATA Interface Signals
65B	ATA_DRQ	I	ATA DMA request
66B	/ATA_IOW	O	ATA write
67B	ATA_Isolation	O	ATA write enable for PCI bus sharing
68B	/ATA_DACK	O	ATA DMA acknowledge
			Dedicated PCI Signals
70B	PCI_CLOCK	O	PCI and external peripheral clock
72B	/PCI_REQ	O	PCI bus request
78B	PCI_IDSEL	O	Initial device select
85B	/PCI_FRAME	O	Frame start
86B	/PCI_TRDY	I	Target ready
87B	/PCI_STOP	O	Transition stop
88B	PCI_PAR	O	Bus parity
95B	/PCI_CBE_0	O	Command byte enable 0

Pin Number	Signal	I/O	Comments	
Pin Row X1C				
1C, 2C, 4C, 5C	+3V3	I	Supply voltage +3.3 VDC	
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C	GND	-	Ground 0 V	
6C	VBAT	I	Connection for external battery (+) 2.4 - 3.3 V to supply (backup) the RTC U5	
8C	/WDO	O	External Watchdog output	
9C	/FL_WP	O	Flash Write Protection (only with P33 Flash populated)	
10C	/SRESET	I/O	External SRESET is an open drain signal which is connected to a 10 kOhm pull-up resistor on the module. Assertion of SRESET causes assertion of the internal soft reset. Internal soft reset is actually an interrupt that takes the same exception vector as HRESET. In particular, this means that SRESET cannot abort a hung XLB operation, and no device should use SRESET in a way that interferes with any bus operation in progress. SRESET can also be asserted by internal sources. When SRESET is asserted internally, external SRESET is also asserted.	
11C	/HRESET	I/O	HRESET is a bi-directional signal with a Schmitt-trigger input and an open drain output. The HRESET signal is connected a 10 kOhm pull-up resistor on the module. Assertion of external HRESET causes external HRESET and SRESET as well as internal hard and soft resets to be asserted for at least 4096 reference clock cycles. During PORRESET or HRESET the reset configuration word is sampled to establish the initial state of various vital internal MPC5200B functions. The reset configuration word is latched internally when PORRESET or HRESET is released.	
13C	AC97_1_RES	O	AC97 Codec Signals (PSC1) Reset signal to the external AC97 device	
14C	AC97_1_SYNC	O		Frame sync, or start-of-frame (SOF)
15C	AC97_1_BITCLK	I		Driven by the external serial bit-clock
16C	AC97_1_SDATA_IN	I		AC97 serial data input
18C	CAN2_TX	O	CAN transmit output of the second CAN interface (PSC2)	
19C	UART6_RXD_TTL	I	PSC6 receive data signal	
20C	UART6_TXD_TTL	O	PSC6 transmit data signal	
21C	RXD6_232	I	RxD input on the RS-232 transceiver for the MPC UART (PSC6)	

Pin Number	Signal	I/O	Comments
23C	TXD6_232	O	TxD output on the RS-232 transceiver for the MPC UART (PSC6)
24C	UART6_RTS_TTL	I	PSC6 request to send signal
25C	UART6_CTS_TTL	O	PCS6 clear to send signal
Second I²C Interface			
26C	I2C2_CLK	I/O	Clock (SCL)
28C	I2C2_IO	I/O	Data (SDA)
31C	I2C1_CLK	I/O	Clock for first I2C-Interface (SCL)
10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are NC)			
29C	ETH_DUPLEX	O	Duplex LED (H=half duplex, L=full duplex)
30C	ETH_NWAYEN	O	Collision LED (H = no collision, L = collision detected)
33C	ETH_LINK	O	Link/Activity LED (L=link; toggle=act)
34C	ETH_SPEED	O	Speed LED (H=10 Mbit/s, L=100 Mbit/s)
35C	ETH_RX-	I	Differential receive input
36C	ETH_TX-	O	Differential transmit output
38C	/ETH_PD	I	Power down
JTAG Interface			
39C	/COP_TRST	I	JTAG reset input. Via logic OR connected to /PORRESET resulting in /CPU_TRST signal.
40C	CK_STOP	O	Scan enable, clock stop
41C	/CPU_TRST	I/O	JTAG reset in/output
43C	PSC2_4	I/O	Freely available GPIO with wakeup function
44C	Timer5	I/O	Timer 5 signal of the MPC5200B
USB1 (Host)			
45C	USB1_OVRCRNT	I	Over current
46C	USB1_SUSPEND	O	Suspend
48C	USB1_RXN	I	Receive negative
49C	USB1_TXN	O	Transmit negative
50C	USB1_OE	O	Output enable (active high)
MII Signal Interface			
51C	ETH_RXD3	I	Receive Data Input 3
53C	ETH_RXD1	I	Receive Data Input 1
54C	ETH_RXD0	I	Receive Data Input 0
55C	ETH_COL	I	Collision Detect Input
56C	ETH_RXDV	I	Receive Data Valid
58C	ETH_TXERR	O	Transmit Error Output
59C	ETH_TXD2	O	Transmit Data Output 2
Misc. Signals			
60C	Timer6	I/O	Timer 6 Signal of MPC5200B
61C	Timer4	I/O	Timer 4 Signal of MPC5200B

Pin Number	Signal	I/O	Comments
FPGA IO Signals			
63C	FPGA_B2_A12	I/O	
64C	FPGA_B2_B12	I/O	
65C	FPGA_B2_A14	I/O	
66C	FPGA_B2_B14	I/O	
68C	FPGA_B2_D7	I/O	
69C	FPGA_B3_C14	I/O	
70C	FPGA_B3_C15	I/O	
71C	FPGA_B3_D13	I/O	
73C	FPGA_B3_D16	I/O	
74C	FPGA_B3_E14	I/O	
75C	FPGA_B3_E15	I/O	
76C	FPGA_B3_F13	I/O	
78C	FPGA_B3_F16	I/O	
79C	FPGA_B3_G13	I/O	
80C	FPGA_B3_G15	I/O	
81C	FPGA_B3_H11	I/O	
83C	FPGA_B3_H15	I/O	
84C	FPGA_B3_J12	I/O	
85C	FPGA_B3_J15	I/O	
86C	FPGA_B3_K13	I/O	
88C	FPGA_B3_L12	I/O	
89C	FPGA_B3_L15	I/O	
90C	FPGA_B3_L16	I/O	
91C	FPGA_B3_M14	I/O	
93C	FPGA_B3_N12	I/O	
94C	FPGA_B3_N16	I/O	
95C	FPGA_B3_P14	I/O	
96C	FPGA_B3_P16	I/O	
98C	FPGA_B4_N6	I/O	
99C	FPGA_B4_P6	I/O	
100C	FPGA_B4_R6	I/O	
Pin Row X1D			
1D, 2D	+3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	GND	-	Ground 0 V
4D, 5D	FPGA_VCCIO	-	Optional IO-Voltage for FPGA Banks 1, 2, and 3
6D	VCC_SRAM	O	VCC_SRAM supply voltage is generated by VBAT or +3V3 using a battery backup circuit (MAX6364). VCC_SRAM serves as supply voltage for the Real-Time Clock and for the SRAM.
7D	/PWR_Good	O	Power Good Open Drain Output of the supervisor circuit

Pin Number	Signal	I/O	Comments
8D	WDI	I	Watchdog Input Signal
10D	/PorReset	I	Reset input signal of the MPC5200B-I/O. It could be asserted via connection to a reset push button. Signal connected to +3V3 via 10 kOhm pull-up resistor.
11D	GPIO_WKUP_7	I/O	Dedicated GPIO with wakeup capability
12D	Timer2	I/O	Timer 2 signal of the MPC5200
13D	Timer3	I/O	Timer 3 signal of the MPC5200
15D	AC97_1_SDATA_O UT	O	AC97 codec signal (PSC1) AC97 serial data output
16D	UART3_RXD_TTL	I	PSC3 receive data signal
17D	UART3_TXD_TTL	O	PSC3 transmit data signal
18D	CAN2_RX	I	CAN receive of the second CAN interface (PSC2)
20D	CAN1_RX	I	CAN receive of the first CAN interface (PSC2)
21D	CAN1_TX	O	CAN transmit of the first CAN interface (PSC2)
22D	RXD3-232	I	RxD input on the RS-232 transceiver for UART3 (PSC3).
23D	TXD3-232	O	TxD output on the RS-232 transceiver for UART3 (PSC3).
25D	UART3_RTS_TTL	I	PSC3 request to send signal
26D	UART3_CTS_TTL	O	PCS3 clear to send signal
27D	SPI_MOSI	I/O	SPI Interface (PSC3) SPI master out slave in SPI master in slave out SPI clock SPI slave select
28D	SPI_MISO	I/O	
30D	SPI_CLK	I/O	
31D	SPI_SS	O	
32D	I2C1_IO	I/O	Data line of first I ² C interface (SDA)
33D	/IRQ_RTC	O	Interrupt from the on-board RTC U5. Interrupt can be programmed to occur to a specific time or date.
35D	ETH_RX+	I	10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are NC) Differential receive input Differential transmit output MII interface interrupt
36D	ETH_TX+	O	
37D	/ETH_INT	O	
38D	CPU_TCK	I	MPC5200B JTAG interface Clock Data in Data out Mode select
40D	CPU_TDI	I	
41D	CPU_TDO	O	
42D	CPU_TMS	I	
43D	USB1_PORTPWR	O	USB1 (Host) Enable/disable port power Speed select Receive data Receive positive Transmit positive
45D	USB1_SPEED	O	
46D	USB1_RXD	I	
47D	USB1_RXP	I	
48D	USB1_TXP	O	

Pin Number	Signal	I/O	Comments
			MII Interface Signals
50D	ETH_CRS	I	Carrier Sense Input
51D	ETH_RXERR	I	Receive Error Input
52D	ETH_RXD2	I	Receive Data Input 2
53D	ETH_TXCLK	I	Transmit Clock
55D	ETH_RXCLK	I	Receive Clock
56D	ETH_MDIO	I/O	Management Data I/O
57D	ETH_MDC	O	Management Data Clock
58D	ETH_TXD3	O	Transmit Data Output 3
60D	ETH_TXD1	O	Transmit Data Output 1
61D	ETH_TXD0	O	Transmit Data Output 0
62D	ETH_TXEN	O	Transmit Enable
63D	FL_Bank_Sel	I	Flash Bank Selection Selection of Flash Bank if P33 Flash is populated
			FPGA IO Signals
65D	FPGA_B2_C12	I/O	
66D	FPGA_B2_C13	I/O	
67D	FPGA_B2_A13	I/O	
68D	FPGA_B2_B13	I/O	
70D	FPGA_B3_C16	I/O	
71D	FPGA_B3_D14	I/O	
72D	FPGA_B3_D15	I/O	
73D	FPGA_B3_E13	I/O	
75D	FPGA_B3_E16	I/O	
76D	FPGA_B3_F14	I/O	
77D	FPGA_B3_F15	I/O	
78D	FPGA_B3_G12	I/O	
80D	FPGA_B3_G16	I/O	
81D	FPGA_B3_H12	I/O	
82D	FPGA_B3_H13	I/O	
83D	FPGA_B3_J11	I/O	
85D	FPGA_B3_J16	I/O	
86D	FPGA_B3_K15	I/O	
87D	FPGA_B3_K16	I/O	
88D	FPGA_B3_L14	I/O	
90D	FPGA_B3_M12	I/O	
91D	FPGA_B3_M15	I/O	
92D	FPGA_B3_M16	I/O	
93D	FPGA_B3_N15	I/O	
95D	FPGA_B3_P15	I/O	
96D	FPGA_B4_K6	I/O	
97D	FPGA_B4_K7	I/O	
98D	FPGA_B4_N7	I/O	
100D	NC	-	Not connected

Table 2: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-MPC5200B-I/O has 12 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* and indicates the location of the jumpers on the board.

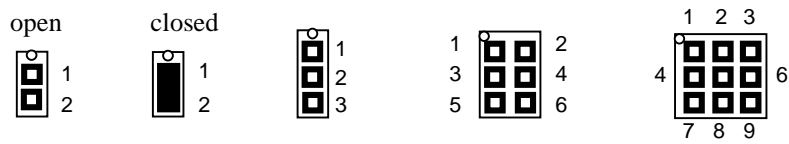
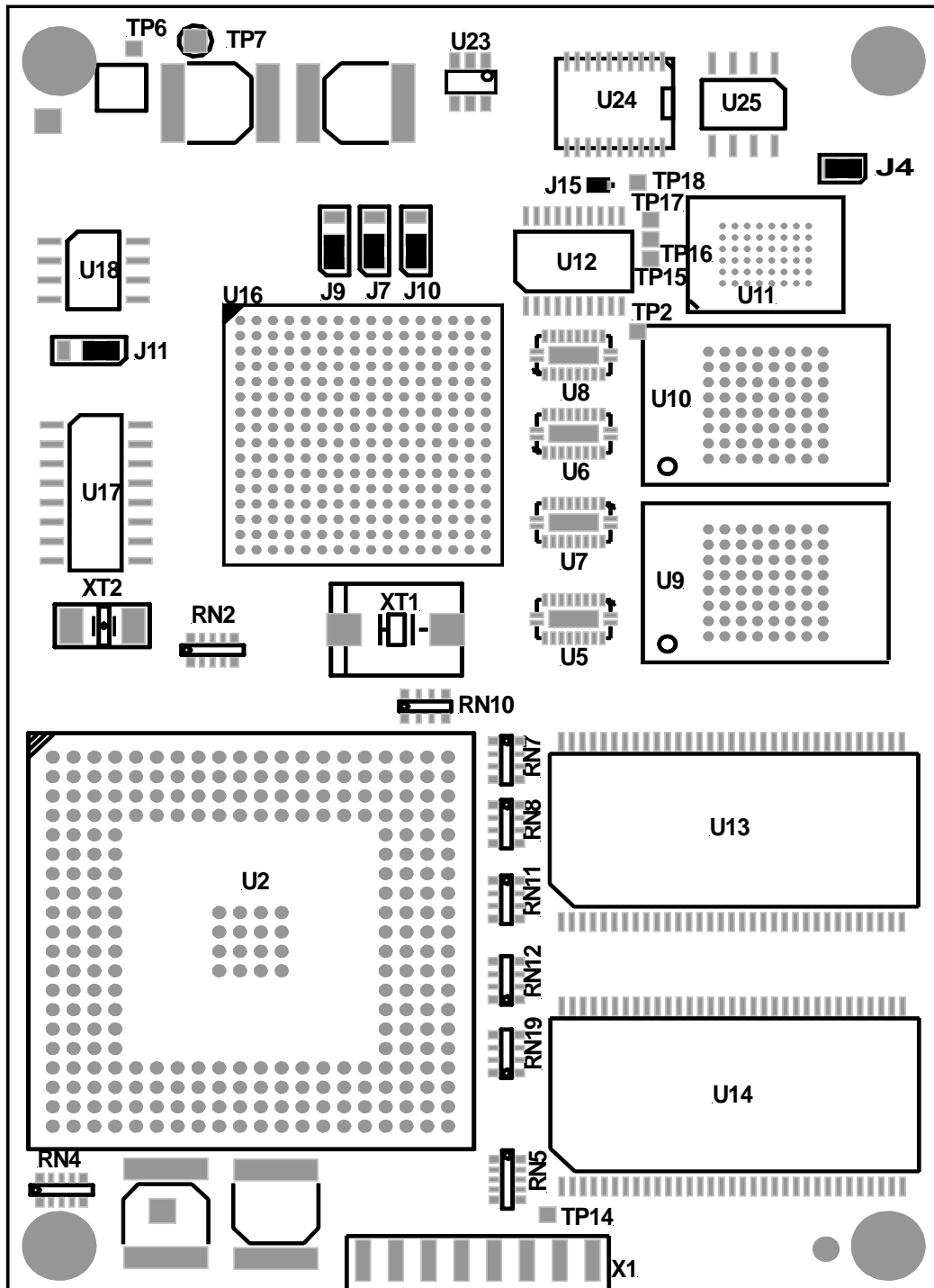


Figure 5: Numbering of the Jumper Pads



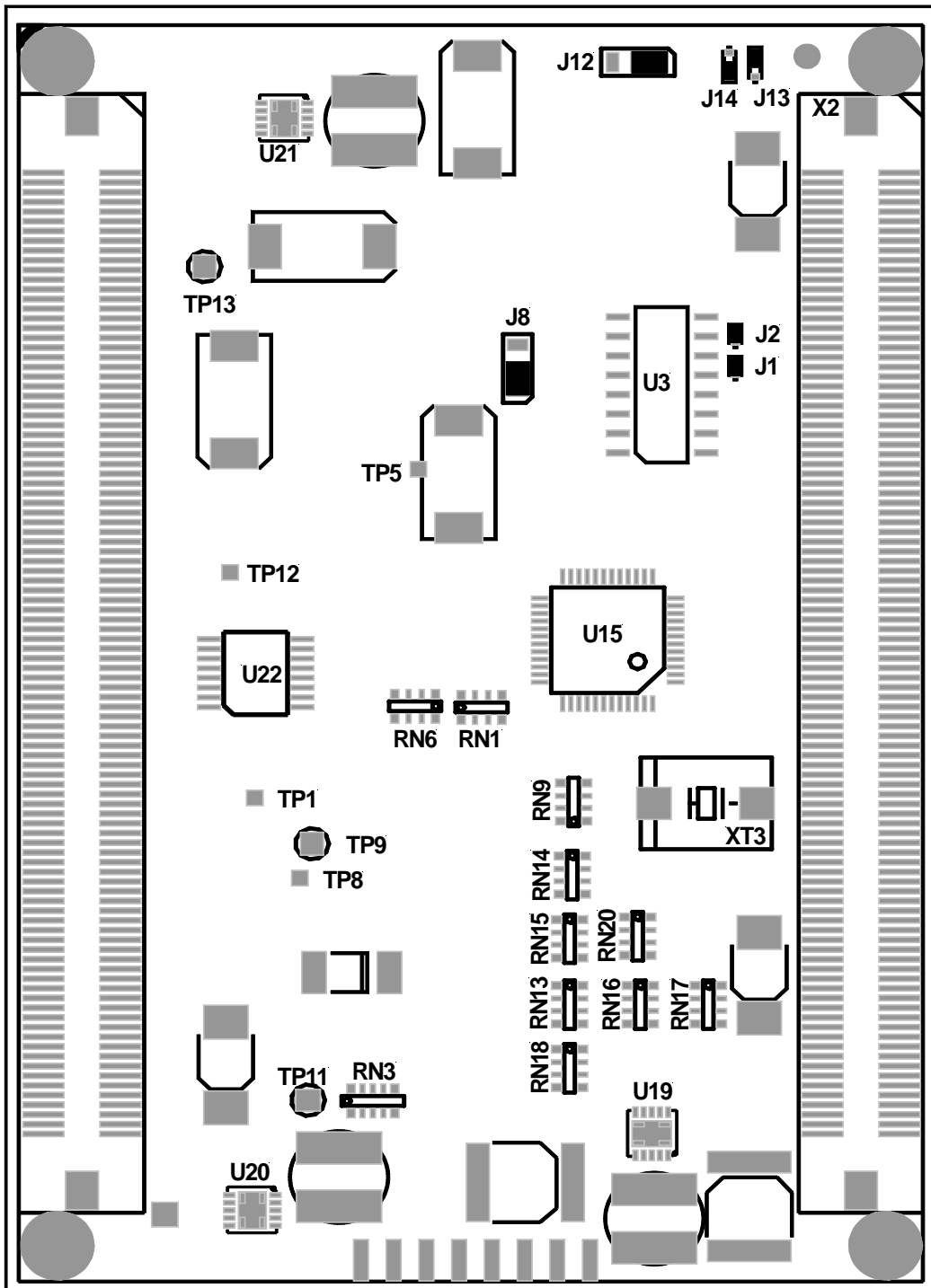


Figure 6: Location of the Jumpers)
 (phyCORE-MPC5200B-I/O Standard Version)

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
J1, J2		J1 and J2 disconnect the receive lines (UART3_RXD_TTL and UART6_RXD_TTL) of the MPC5200B PSC3 and PSC6 from the RS-232 transceiver at U3. This makes the controller's TTL signals available at pins X1D16 (UART3_RXD_TTL) and X1C19 (UART6_RXD_TTL). This is useful, for instance, for optical isolation of the RS-232 interface.
open		The UART receive signals UART3_RXD_TTL and UART6_RXD_TTL are disconnected from the RS-232 transceiver.
closed	X	The UART receive signals UART3_RXD_TTL and UART6_RXD_TTL are connected to the on-board RS-232 transceiver.
Package Type		0R in SMD 0805
J4		J4 connects pin 7 of the serial memory at U25 to GND. On many memory devices pin 7 enables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCORE-MPC5200B-I/O will have this write protection function. <i>Please refer to the corresponding memory data sheet for more detailed information.</i>
open		
closed	X	
Package Type		0R in SMD 0805
J8		J8 configures the FPGA configuration mode <i>Please refer to the corresponding FPGA Data Sheet for more detailed information.</i>
1 + 2	X	The FPGA configuration mode is set to Passive Serial Mode (PS Mode). This allows loading the FPGA firmware through a controller interface. In this configuration an external FPGA configuration EEPROM is not required.
2 + 3		The FPGA configuration mode is set to Active Serial Mode (AS mode). In order to use this configuration an external FPGA configuration EEPROM is required at U18 from which the functional implementation can be loaded into the FPGA.
Package Type		0R in SMD 0805
J7, J9, J10		Each of these jumpers configures the I/O voltage of the corresponding freely available FPGA I/O banks. <i>Please refer to the corresponding FPGA Data Sheet for more detailed information about the I/O bank voltages.</i>
1 + 2	X	I/O voltage of the corresponding FPGA bank set to 3V3 supply voltage.
2 + 3		I/O voltage of the corresponding FPGA bank supplied by an external source through the FPGA_VCCIO input.
Package Type		0R in SMD 0805

Jumper	Default	Comment
J11		J11 configures the use of the PSC6 signals from the MPC5200B. <i>Please refer to the corresponding controller Data Sheet for more detailed information.</i>
1 + 2	X	The GPIO6 signal is connected to the select input of the multiplexer IC at U17. This allows configuration of the PSC6 signals in two different configurations: 1. GPIO6 goes low: This multiplexer configuration allows use of the PSC6 I/O signals as UART interface. The multiplexer at U17 will route the PSC6 I/O signals to the RS-232 transceiver. 2. GPIO6 goes high: In this multiplexer configuration the FPGA contents can be configured using the PSC6 I/O signals.
2 + 3		The PSC6 I/O signals are directly connected to the FPGA configuration interface through the multiplexer at U17.
Package Type		0R in SMD 0805
J13, J14		J5 and J6 define the slave addresses (A1 and A2) of the serial memory U4 on the I ² C2 bus. In the high-nibble of the address, I ² C memory devices have the slave ID 0xA. The low-nibble consists of A2, A1, A0, and the R/W bit. A0 is tied to GND. It must be noted that the RTC at U5 is also connected to the I ² C bus. The RTC has the address 0xA2/0xA3 which cannot be changed.
1 + 2, 2 + 3	X	A2= 0, A1= 0, A0= 0 (0xA0 / 0xA1) I ² C slave address 0xA0 for write operations and 0xA1 for read access.
1 + 2, 1 + 2		A2= 1, A1= 0, A0= 0 (0xA8 / 0xA9)
2 + 3, 2 + 3		A2= 0, A1= 1, A0= 0 (0xA4 / 0xA5)
2 + 3, 1 + 2		A2= 1, A1= 1, A0=0 (0xAC / 0xAD)
Package Type		0R in SMD 0805
J12		Enables or disables the clock output of the I ² C RTC U5 RTC clockout is connected to X1B1.
1 + 2	X	RTC clockout disabled
2 + 3		RTC clockout enabled
Package Type		0R in SMD 0805
J15		J15 configures the /CS signal used for accessing the Flash.
open		If J15 is not populated, then a programmed GAL ATF16LV8C must populate U12 in order to ensure proper functioning of the phyCORE module. The GAL will generate the Flash /CS signal based on its input signals.
closed	X	If J15 is populated, then the Flash /CS signal is directly connected to the controller's /CS0 signal. The user has to ensure that only one of these options is used. Having both J15 and U12 installed at the same time is not allowed.
Package Type		0R in SMD 0402

Table 3: Jumper Settings

4 Power Requirements

The phyCORE-MPC5200B-I/O only requires one main supply voltage:

Supply voltage: +3.3 V \pm 10 % with 1.5 A load

Caution:

Connect all +3V3 input pins to your power supply and at least the matching number of GND pins neighboring the +3V3 pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry

Optional Supply Input VBAT

VBAT is the input pin that supplies the Real-Time Clock (U5). The MAX6364 battery supervisor IC (U12) senses the 3.3 V main supply and VBAT and switches to the voltage with the higher level. VBAT should be supplied from a 3 V source (i.e. lithium battery).

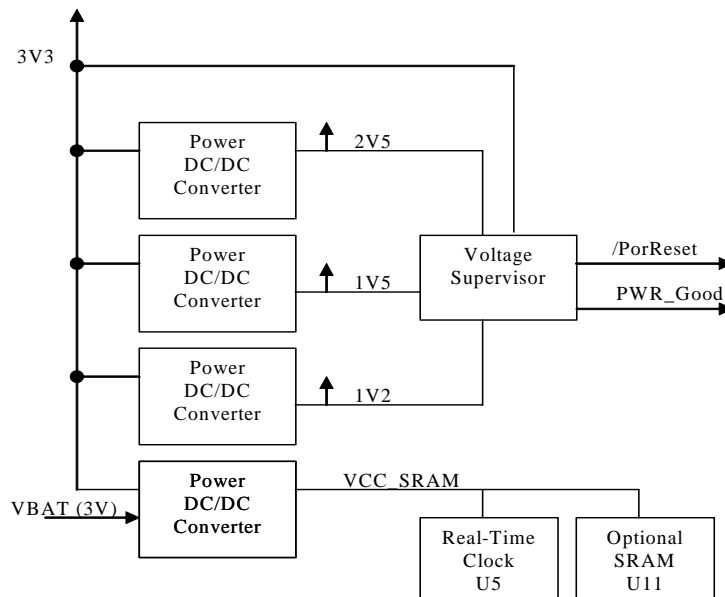


Figure 7: Power Supply Diagram

Internally generated voltages: 1V2, 1V5, 2V5

- 3 V3 PowerPC I/O, FPGA I/O, Flash memory
- 2 V5 DDR SDRAM and Ethernet PHY
- 1 V5 PowerPC Core
- 1 V2 FPGA Core and FPGA PLL

4.1 Voltage Supervision and Reset

The input voltage 3V3 as well as the on-board generated operation voltages 2V5 and 1V5 are monitored by a voltage supervisor device at U22. This circuitry is responsible for generation of the system reset signal /PorReset. The voltage supervisor IC initiates a reset cycle if any operating voltage drops below its minimum threshold value. After all voltages reach their required value, the supervisor chip adds an additional 200 ms delay until the /PorReset line will be inactive (high). /PorReset connects to the processor reset input.

/PorReset is combined via the diodes D7 and D6 with /COP_TRST to a logic OR with /CPU_TSRT (JTAG controller reset) as output. This logic connection is used to ensure a proper reset of the CPU internal debug interface by /PorReset or by the COP signal /COP_TRST.

The /PorReset signal can be used in order to force a reset of the phyCORE-MPC5200B-I/O module by an external source. The /PorReset signal can be considered as both an input and an output. In order to release a proper reset, the /PorReset signal should be pulled to GND for the duration of the reset via an open collector circuit.

5 System Start-Up Configuration

During the reset cycle the MPC5200B processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitry (pull-up or pull-down resistors) is located on the phyCORE module.

The system start-up configuration includes:

- Clock configuration
- Basic LocalPlus characteristic for boot memory configuration

The following default configuration is read by the processor with the rising edge of the reset line /PorReset. The logic level of the signals written in *italic style* could be configured via solder jumpers on-board (*refer to section 3*).

Signal Name	Register Bit	Logic Level	Description
/LP_Ale LP_RD/WR <i>/ATA_low</i> <i>/ATA_lor</i> <i>/ATA_Dack</i>	PPC_pll_cfg [0..4]	0 1 0 0 0	Bus clock ratio XLB: core clock = 1:3 132 MHz * 3 = 396 MHz
/LP_Ts	xlb_clk_sel	0	Bit=0: XLB_CLK = fsystem / 4 Bit=1: XLB_CLK = fsystem / 8
USB1_TXN	sys_pll_cfg0	0	Bit =0: fsystem = 16x SYS_XTAL_IN Bit =1: fsystem = 12x SYS_XTAL_IN
USB1_TXP	sys_pll_cfg1	0	Bit=0: fvcosys = fsystem Bit=1: fvcosys = 2 x fsystem
ETH_TXEN	boot_rom_mg	0	Bit=0: No boot in most graphics mode 1 Bit=1: Boot in most graphics mode
ETH_TXD1	ppc_msrip	1	Bit=0: 0000_0100 (hex) boot address Bit=1: FFF0_0100 (hex) boot address
ETH_TXD2	boot_rom_wait	1	Bit=0: 4 PCI bus clocks of wait state Bit=1: 48 PCI bus clocks of wait state
ETH_TXD3	boot_rom_swap	0	Bit=0: no byte lane swap, same endian ROM image Bit=1: byte lane swap, different endian ROM image
ETH_TXERR	boot_rom_size	1	Boot ROM address is max 25 significant bits during address tenure. Bit=0: 16-bit ROM data bus Bit=1: 32-bit ROM data bus
ETH_MDC	boot_rom_type	1	Bit=0: non-muxed boot ROM bus, single tenure transfer Bit=1: muxed boot ROM bus, with address and data tenures, ALE and TS active.
ETH_TXD0	large_flash_sel	0	Bit=0: No boot in large Flash mode 1 Bit=1: Boot in large Flash mode 1,3,4

Table 4: System Start-Up Configuration

Note:

Since most of these signal lines are routed to the phyCORE connector care must be taken not to overwrite the startup configuration accidentally when connecting these signals to external devices.

6 System Memory

The standard system memory consist of Flash memory, DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) and a small non-volatile memory device. In addition to the standard memory configuration it is possible to populate a battery-backed SRAM with 16-bit data bus width.

- 32 MByte Intel Strata Flash memory (2x 16-bit, multiplexed mode)
- 64 MByte DDR SDRAM (2x 16-bit)
- 4 kByte serial memory (EEPROM)
- optionales bis zu 2MByte großes 16 bittiges batteriepufferbares RAM

The Flash memory is connected to the PowerPC LocalPlus bus and is controlled by /CS0. This Chip-Select signal is used for boot operation.

The DDR SDRAM is connected to the special SDRAM interface of the MPC5200B processor and operates at the maximum frequency (132 MHz).

Communication to the small non-volatile memory device (EPROM) is established over the processor's I²C bus. This memory device holds the boot loader (U-Boot) environment variables in its first two kilobytes and can be used for parameter storage.

The size of the optional battery-backed SRAM can be up to 2 MByte. This SRAM device at U11 is connected to the MPC5200B LocalPlus bus using a 16-bit data bus with access controlled by the /CS2 signal.

6.1 Flash Memory

Use of Flash as non-volatile memory on the phyCORE-MPC5200B-I/O provides an easily reprogrammable means of code storage.

- 32 MByte Intel Strata Flash memory
- 32-bit bus width
- Only asynchronous operation is possible

The Flash memory bank at U9 and U10 supports the following Intel memory devices:

Type	Size	Manufacturer	Device Code	Manufacturer Code
Asynchronous Devices				
2*28F128J 3	2*16 MByte	Intel	0x0018	0x0089
2*28F256P 33	2*32MByte	Intel		

Table 5: Choice of Flash Memory Devices and Manufacturers¹

¹: Flash types in the shaded lines are the preferred parts for the phyCORE-MPC5200B-I/O.

The organization of the Flash memory bank is 32-bit. The Flash memory bank is controlled by the processor Chip Select signal /CS0. This Chip Select signal is the dedicated control signal for boot purposes.

The MPC5200B's LocalPlus bus can be configured for many different bus modes. For /CS0 the 25-bit address / 32-bit data multiplexed mode was chosen because it offers the largest address space without interfering the ATA or PCI bus. With 25 address lines a total of 32 MByte of data/code can be addressed. It is possible to use different bus modes on other available Chip Select signals.

The Flash memory bank 0 starts at address 0x0000_0100 or 0xFFFF_0100 depending on the startup configuration and relative to the base address of the processor's Chip Select signal /CS0.

The access speed depends on the equipped memory device. The LocalPlus Bus clock cycle is determined by the PCI clock which is configured by the PCI clock divider. A typical configuration selects 66 MHz. The resulting basic cycle time is 15.15 ns. The MPC5200B processor multiplexed read or write is divided into a address tenure and a data tenure. Because the Chip Select signal is generated with the start of the data tenure only this period is of interest for access time calculation.

The equation for access time calculation is: $(2+WS) * t_{\text{PICK}} - 8.5 \text{ ns}$

To support all memory speed grades up to 75 ns at least 4 wait states must be added for /CS0.

- 4 wait states for /CS0 (supports 66 MHz PCI clock)

No additional voltages are needed for in-system programming. As of the printing of this manual, Flash devices generally guarantee at least 100,000 erase/programming cycles. *Refer to the applicable INTEL data sheet for detailed description of the erasing and programming procedure.*

6.2 DDR SDRAM

The phyCORE-MPC5200B-I/O is equipped with fast **Double Data Rate Synchronous Dynamic Random Access Memory** (DDR SDRAM) devices. This memory is connected to a dedicated SDRAM interface provided by the MPC5200B processor.

The DDR SDRAM memory bank at U13 and U14 consists of two 16-bit data port devices connected in parallel to support the 32-bit bus width of the processor. The memory bank is controlled by Chip Select signal /SD_CS0 of the processor's DDR SDRAM controller.

Table 6 shows all possible memory configurations.

Available Capacity	Device Organization	Devices (two)
32 MByte	128 MBit 2 MBit x 16 x 4 banks	MT46V8M16 TSOP66 packaging
64 MByte	256 MBit 4 MBit x 16 x 4 banks	MT46V16M16 TSOP66 packaging
128 MByte	512 MBit 8 MBit x 16 x 4 banks	MT46V32M16 TSOP66 packaging

Table 6: DDR SDRAM Device Selection

6.3 Serial Memory

The phyCORE-MPC5200B-I/O features a non-volatile memory device (EEPROM) with a serial I²C interface. This memory can be used for storage of configuration data or operating parameters that must be maintained in the event of a power interruption. The available capacity is 4 kByte.

Note:

The first 2 kilobytes section of the EEPROM is already used for storing the boot manager (U-Boot) environment variables. This portion must not be used by user data.

The MPC5200B processor provides two on-chip I²C interfaces. The memory device is connected to I²C interface #2.

Table 7 gives an overview of the possible devices for use at U25 as of the printing of this manual.

Type	Size	I ² C Frequency	Address Pins	Write Cycles	Life of Data	Device	Manufacturer
EEPROM	4 kBytes	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC32	CATALYST

Table 7: Serial Memory Options for U25

It is important to note that the RTC U5 is also connected to the I²C #2 bus. The RTC can operate with a bus frequency up to 400 kHz. Therefore the use of high bus frequencies for accessing the serial memory is not recommended. The RTC has the I²C bus slave address 0xA2 / 0xA3. The slave address of the serial memory must be selected accordingly using solder jumpers J5 (A1) and J6 (A2) to avoid bus collision. The address input A0 is hard-wired to GND.

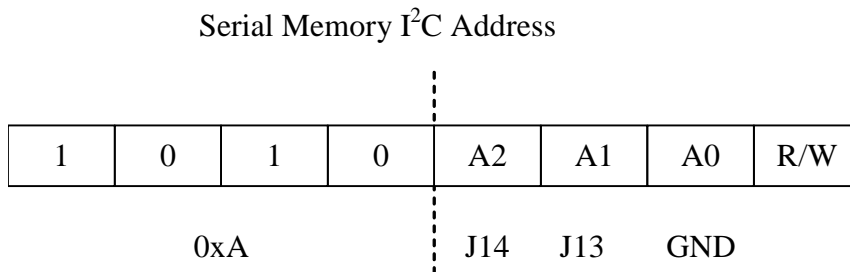


Figure 8: Serial Memory I²C Slave Address

Possible configuration options are shown below:

I ² C Address	J13 A1	J14 A2
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 8: Serial Memory I²C Address (Examples)

Address lines A1 and A2 are not always made available with certain serial memory types. This should be noted when configuring the I²C bus slave address.

6.4 Optional Battery-Backed SRAM

The phyCORE-MPC5200B-I/O can be populated with an optional battery-backed SRAM supporting non-volatile data storage. The use of the backup battery is optional. However, when used without the battery as a backup supply during power down of the phyCORE-MPC5200B-I/O module all data stored in this SRAM device will be lost. The optional SRAM features either 1 MByte or 2 MByte of storage capacity and has a 16-bit data bus connection to the processor.

Note:

With a typical SRAM standby current draw of 5 µA at 3 V and when using a 3V/190mAh Lithium battery, the longest possible backup period would be up to 4 years. Replacement of the backup battery is required at this time.

Access to the battery-backed SRAM is controlled by the processor's Chip Select signal /CS2. However, the Byte Select lines are generated by the GAL ATF16LV8C based on the TSIZ signals from the processor.

Table 9 gives an overview of available SRAM types for use at U11 on the phyCORE-MPC5200B-I/O at the time this manual was created. PHYTEC reserves the right to use alternative SRAM types should they become available in the future.

Type	Capacity	Access Time	Device	Manufacturer
SRAM	1 MByte	55ns/70ns	K6F8016U6M	Samsung
SRAM	2 MByte	55ns/70ns	K6F1616U6C	Samsung
SRAM	2 MByte	45ns	CY62167DV30	Cypress
SRAM	2 MByte	45ns/55ns	HM62V16100	Renesas

Table 9: SRAM Device Options for U11

7 Serial Interfaces

7.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MPC5200B-I/O at U3. This device adjusts the signal levels of the UART3_RXD/TXD_TTL and UART6_RXD/TXD_TTL lines (MPC5200B PSC3/PSC6). The RS-232 interface enables connection of the module to a COM port on a host-PC or other peripheral devices. In this instance, the RXD3-232 or RXD6-232 line (X1D22/X1C21) of the transceiver is connected to the corresponding TXD line of the COM port; while the TXD3-232 or TXD6-232 line (X1D23/X1C23) is connected to the RXD line of the COM port. The Ground circuitry of the phyCORE-MPC5200B-I/O must also be connected to the applicable Ground pin on the COM port.

The processor's on-chip UART supports handshake signal communication. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the module.

Furthermore it is possible to use the TTL signals of both of the UART channels externally. These signals are available at X1D16, X1D17 (UART3_RXD_TTL, UART3_TXD_TTL) and X1C19, X1C20 (UART6_RXD_TTL, UART6_TXD_TTL) on the phyCORE-connector. External connection of TTL signals is required for galvanic separation of the interface signals. Using solder jumpers J1 and J2, the TTL transceiver outputs of the on-board RS-232 transceiver devices can be disconnected from the receive lines UART3_RXD_TTL and UART6_RXD_TTL. This is required so that the external transceiver does not drive signals against the on-board transceiver. The transmit lines UART3_TXD_TTL / UART6_TXD_TTL can be connected parallel to the transceiver input without causing any signal conflicts.

7.2 Ethernet Interface

Connection of the phyCORE-MPC5200B-I/O to the world wide web or a local network (LAN) is possible over the integrated FEC (Fast Ethernet Controller) of the Freescale processor. The FEC operates with a data transmission speed of 10 or 100 Mbit/s.

7.2.1 PHY Physical Layer Transceiver

The phyCORE-MPC5200B-I/O has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED monitoring signals extends to phyCORE-connector X2. In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required 49,9 Ohm +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module.

If you are using the applicable phyCORE-MPC5200B-I/O Carrier Board for the phyCORE-MPC5200B-I/O (part number PCM-973), the external circuitry mentioned above is already integrated on the board (*refer to section 14.3.7*).

The default PHY address configured with the boot-strapping option is 0x1.

Table 10 shows the interface signals for the Ethernet channel.

FEC Channel PHY U2	Pin Function	Location at phyCORE- Connector
ETH_RX+	Differential positive receive input signal	X1D35
ETH_RX-	Differential negative receive input signal	X1C35
ETH_TX+	Differential positive transmit output signal	X1D36
ETH_TX-	Differential negative transmit output signal	X1C36
ETH_LINK	Link/activity LED output "H"/LED off no link "L"/LED on link "toggle"/LED toggle activity	X1C33
ETH_SPEED	Speed LED output "H"/LED off 10BT "L"/LED on 100BT	X1C34
ETH_DUPLEX	Duplex LED output "H"/LED off Half Duplex "L"/LED on Full Duplex	X1C29
ETH_NWAYEN	Collision LED output "H"/LED off no collision "L"/LED on collisions	X1C30

Table 10: Signal Definition PHY Ethernet Port (U2)

7.2.2 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a **unique** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MPC5200B is located on the bar code sticker attached to the module. This number is a 12-position HEX value.

7.3 USB 1.1 Host Interface

The MPC5200B integrates a USB 1.1 compliant host interface with two ports. This interface supports full-speed (12 Mbit/s) transmission rates. The USB 1.1 controller is integrated in the MPC5200B processor. The physical layer transceiver unit must be connected externally, it is **not** populated on the phyCORE module.

For additional information of the USB 1.1 controller refer to the MPC5200B Reference Manual as well as the USB 1.1 bus specification provided by www.usb.org.

8 The On-Board FPGA

The phyCORE-MPC5200B-I/O SBC module design includes an ALTERA EP2C8 FPGA, which can be used in a variety of applications. Data exchange between the FPGA and the MPC5200B processor occurs over the multiplexed LocalPlus Bus.

8.1 FPGA Bus Connection

As previously mentioned the FPGA is connected to the processor via the multiplexed LocalPlus Bus of the MPC5200B. This connection is used for data transfer between the two components and allows a data exchange of up to 44 Mbyte/s depending on the bus frequency used.

The following LocalPlus Bus signals are routed to the FPGA:

Processor Signal	FPGA Pin
/HRESET	B4_N9
/LP_CS3	B4_N10
/LP_CS4	B4_T11
/LP_ALE	B4_R11
/LP_OE	B4_L9
LP_RD/WR	B4_L10
LP_ACK	B4_R10
/LP_TS	B4_T10
EXT_AD0	B4_K11
EXT_AD1	B4_K10
EXT_AD2	B4_P12
EXT_AD3	B4_P13
EXT_AD4	B4_T12
EXT_AD5	B4_R12
EXT_AD6	B4_T13
EXT_AD7	B4_R13
EXT_AD8	B4_T14
EXT_AD9	B4_R14
EXT_AD10	B4_M11
EXT_AD11	B4_L11
EXT_AD12	B4_N11
EXT_AD13	B4_P11
EXT_AD14	B4_T3
EXT_AD15	B4_R3
EXT_AD16	B4_P5
EXT_AD17	B4_P4
EXT_AD18	B4_T4
EXT_AD19	B4_R4
EXT_AD20	B4_T5
EXT_AD21	B4_R5
EXT_AD22	B4_T7
EXT_AD23	B4_R7
EXT_AD24	B4_L7
EXT_AD25	B4_L8
EXT_AD26	B4_T8
EXT_AD27	B4_R8
EXT_AD28	B4_T9
EXT_AD29	B4_R9
EXT_AD30	B4_N8
EXT_AD31	B4_T6

Table 11: Signal Connection between MPC5200B and FPGA Pins

8.2 FPGA Configuration Interface

The phyCORE-MPC5200B-I/O provides two options for configuring the FPGA. Jumper J8, which is used to configure the FPGA's serial programming interface, is used to select the different options (*refer to section 3 for more details*).

8.2.1 Configuration via Processor GPIO Interface

The phyCORE-MPC5200B-I/O offers the capability of configuring the FPGA over the processor's GPIO signals. In order to use this method, the FPGA's configuration interface must be connected with the applicable GPIO signals on the processor. The analog multiplexer IC at U17 is provided to accomplish this task. In addition, Jumper J11 on the module allows fixed or flexible configuration of the analog multiplexer U17. If the flexible configuration option is selected, the processor's GPIO6 signal is used to configure the analog multiplexer from user software. This allows the user to switch between using the corresponding GPIO signals for either programming the FPGA at runtime or to use the signals with the alternative function depending on the application requirements.

8.2.2 Configuration via Serial Configuration Device

As an alternative to configuring the FPGA via the processor's GPIOs, it is also possible to configure the FPGA using a serial configuration device from ALTERA (e.g. EPCS4). The difference to the variant described in *section 8.2.1* is that the contents of the FPGA can only be changed over the JTAG interface of the FPGA or by exchanging the contents of the serial configuration device. A corresponding initialization of the FPGA is started following power up of the phyCORE-MPC5200B-I/O. Subsequent reconfiguration via software is no longer possible. The FPGA's contents are retained until the next power down.

8.3 FPGA JTAG Interface

The FPGA provides a JTAG interface for convenient programming and testing during the development stage of the corresponding FPGA firmware. The JTAG programming method is always prioritized over all other means of loading code to the device. This means that firmware previously loaded in the FPGA will be overwritten by a JTAG programming cycle.

When using ALTERA's proprietary serial configuration devices in order to program the FPGA it is possible to download firmware to this configuration device over the JTAG interface of the FPGA. The JTAG interface signals of the FPGA are routed to the Molex connectors of the phyCORE-MPC5200B-I/O (*refer to section 2*). When used in combination with the phyCORE-MPC5200B-I/O Carrier Board access to the JTAG port is available at a 10-pin header connector (X8), *refer to section 14.3.14 for details*.

9 The U-Boot Boot Loader

"U-Boot" is a universal boot loader firmware based on GPL (Gnu Public License). Its main function is initializing the system hardware following a reset followed by starting application software such as an operating system.

Furthermore, U-Boot provides various functions to query system information and to change the start-up behavior of the target system. For example U-Boot allows to choose from different boot sources (such as Ethernet, etc.). It also provides functions to download application code into Flash.

The serial interface is used to communicate with U-Boot on the target system. The U-Boot for phyCORE-MPC5200B tiny uses PSC3 with 115,200 Baud, 8, N, 1. The U-Boot boot messages can be viewed within a terminal program running on a host PC using the above mentioned communication settings.

Note:

PHYTEC delivers all phyCORE-MPC5200B-IO modules with a pre-installed U-Boot allowing the user immediate startup. The U-Boot software project is subject to continuous maintenance and improvements. Firmware updates will occur without special notification. Should you require a specific version of U-Boot pre-installed at time of delivery please contact PHYTEC's sales department.

If U-Boot is used as boot loader firmware and basic component of the system software, the user should be familiar with the following topics in order to ensure proper function:

- U-Boot default system configuration
- system resources required by U-Boot
- modifying the U-Boot loader

9.1 U-Boot Default System Configuration

The U-Boot boot loader changes the following default settings to different than the reset values of the processor on the phyCORE-MPC5200B-I/O:

Clock:

Core = 396 MHz, IPB = 132 MHz, PCI = 33 MHz

Memory Base Address Register (MBAR):

0xF0000000

DDR-RAM:

Automatic storage size detection; start address 0x0

Flash:

Chip Select = /CSBoot, 32-bit data bus width, 25 address lines, multiplexed mode, 4 wait states; 32 MByte starting at address 0xFE000000

FPGA:

Chip Select = /CS3 and /CS4, 32-bit data bus width, 25 address lines, multiplexed mode, 32MByte Address space per CS-signal at address 0xE2000000(/CS3) and 0xE4000000(/CS4)

PSC2:

CAN1&2

PSC3 :

UART, 115200 baud, 8,N,1 ; SPI

PCI :

enabled

Ethernet :

100 Mbit/s with MD

I²C_2:

EEPROM at address 0x52, RTC at address 0x51

9.2 System Resources Required by U-Boot

U-Boot is located at address 0xFFF0 0000 in the module's Flash and occupies two sectors (2x 128kByte). The boot loader itself makes sure that these sectors are protected using the Flash's "locked sector" mechanism. This makes accidental erasure of U-Boot almost impossible. Following a system start at address 0xFFF0 0100 (high boot), U-Boot first initializes the DDR-RAM interface, then copies itself to the upper end of the RAM memory space and transfers program execution to this address. As a result U-Boot now runs out of RAM which allows for reprogramming itself in Flash (firmware update).

So called environment variables are used to configure U-Boot. Such variables define the IP number as well as the MAC address using Ethernet configuration as example. The variables are saved in the module's EEPROM (U4) and occupy the first 2 kByte.

When using the RAM memory, care should be taken to not overwrite the U-Boot code as well as the trap table which is located in the lower portion of the RAM. Among other factors, the size of the U-Boot stack determines how much memory at the upper end of the RAM memory range is occupied by U-Boot. As U-Boot is used the stack size is growing and more memory space is required. It is recommended to reserve a sufficient RAM portion to be used for the stack beginning at the stack start address.

9.2.1 The "Backup" U-Boot

In the event the "original" U-Boot at address 0xFFF0 0000 becomes corrupted (e.g. by overwriting the loader with a wrong version) a second U-Boot loader at address 0xFE00 0000 is available as an "emergency" backup version providing the same functionality as the original copy. This backup U-Boot can be started by connecting a 4.7kOhm pull-down resistor at pin X1-C8 during a hardware reset cycle.

Note:

When using the phyCORE-MPC5200B-I/O in conjunction with the applicable Carrier Board (part number PCM-973) the "Backup" U-Boot loader can be started by closing Jumper JP3 at position 1+2.

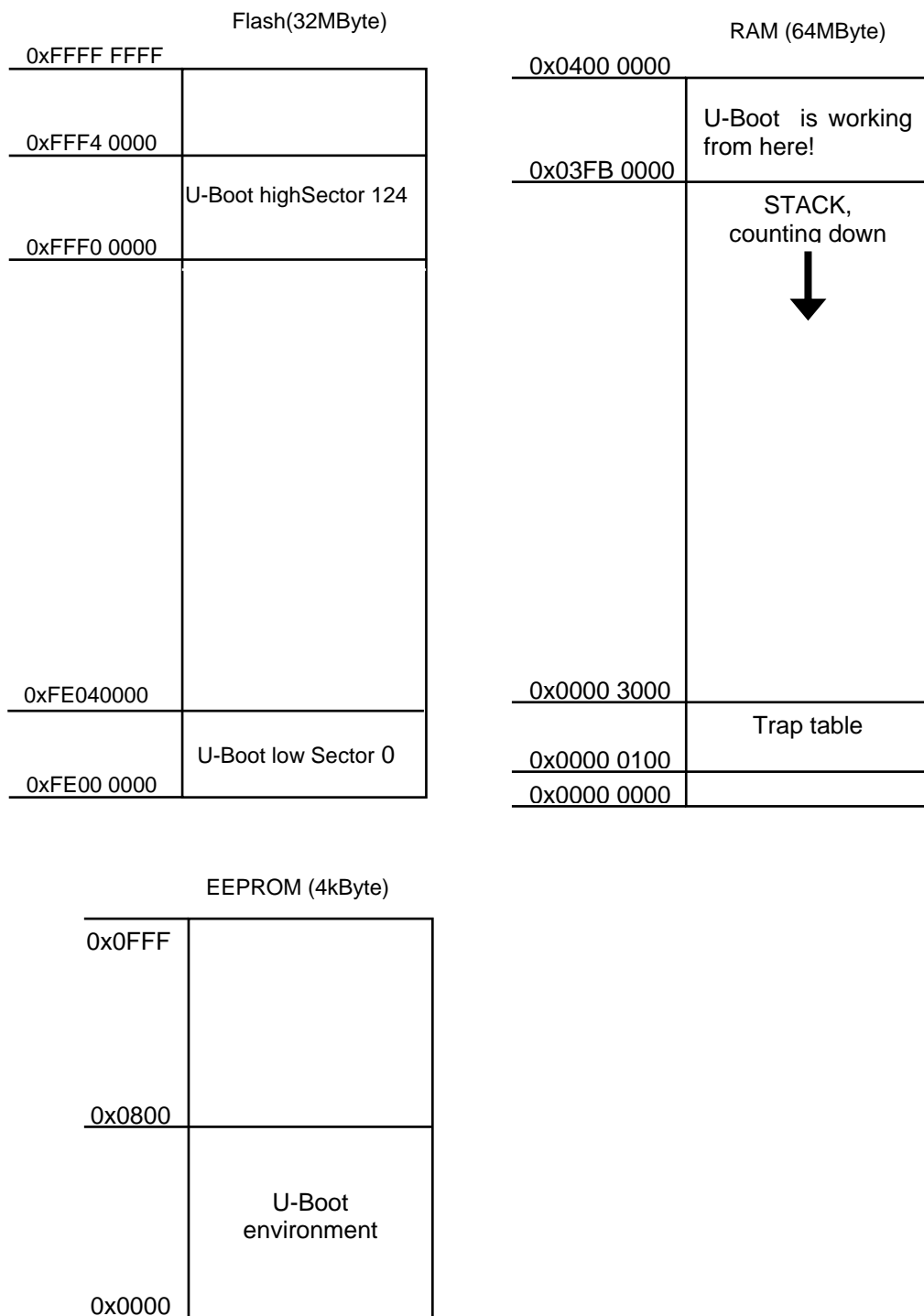


Figure 9: U-Boot Memory Map

9.3 Modifying the U-Boot Loader

Changing the U-Boot should always be compared to recompiling the program code and updating the Flash contents. A detailed description of each individual step would by far exceed the scope of this Hardware Manual. Please refer to the Application Note "Configuring and Updating the Boot Loader", document number LAN-044 for more details.

10 JTAG Interface

The MPC5200B CPU provides a JTAG interface for connecting to debuggers, emulators and boundary scan. The JTAG interface signals extend to the module's phyCORE-connector. Furthermore, there is an on-board JTAG connector (X1) located at the edge of the module, which has the standard COP-Interface pinout but uses a 2.0 mm pin pitch instead of 2.54 mm. The connector is not populated on the standard version of the phyCORE-MPC5200B-I/O. You can order a specific debug version of the module (denoted by the -D part number extension) or populate a 2*8-pin header connector at space X1. The numbering scheme is depicted on the phyCORE-MPC5200B-I/O. The pinout of the JTAG interface at X1 is described in the following table.

Signal	Pin Row		Signal
	Bottom	Top	
TDO	1	2	NC (quack)
TDI	3	4	/TRST
NC (/halted)	5	6	3V3
TCK	7	8	NC
TMS	9	10	NC
/SReset	11	12	GND
/HReset	13	14	NC (key)
CK_Stop	15	16	GND

Table 12: JTAG Interface X1

11 Technical Specifications

The physical dimensions of the phyCORE-MPC5200B-I/O are represented in *Figure 10*.

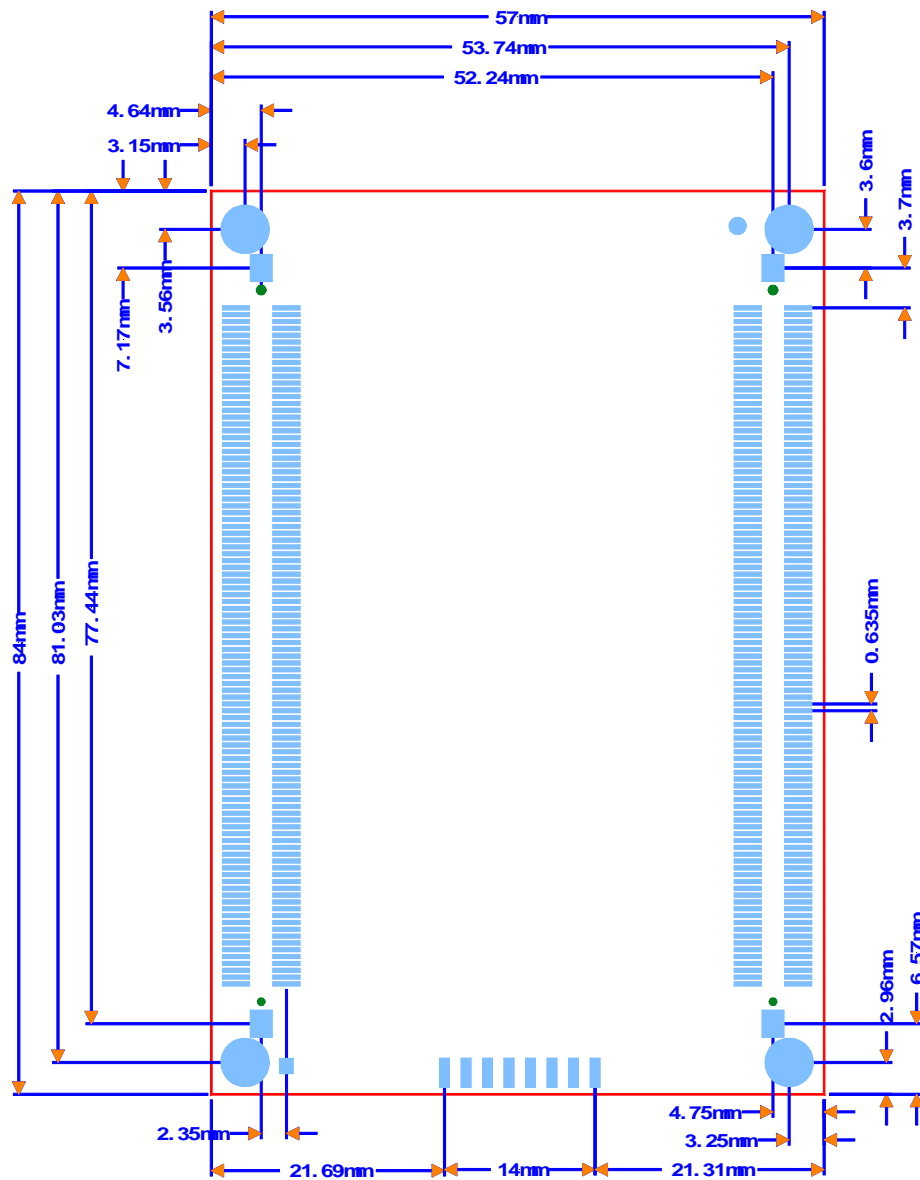


Figure 10: Physical Dimensions (Top View)

The height of all components on the top side of the PCB is ca. 2.5 mm. The PCB itself is approximately 1.6 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 3.0 mm.

Additional Technical Data:

Parameter	Condition	Characteristics
Dimensions		84 mm x 53 mm
Weight		approximately 30g with all optional components mounted on the circuit board
Storage Temp. Range		-40°C to +90°C
Operating Temp. Range:		
Extended		-25°C to +85°C
Humidity		max. 95 % RH not condensed
Operating voltages:		
3.3V supply voltage		3.3 V \pm 5 %
Operating Power Consumption:	(depending on load)	
3.3V supply voltage		Max. 3.3 watts

Table 13: Technical Data

These specifications describe the standard configuration of the phyCORE-MPC5200B-I/O as of the printing of this manual.

Connectors on the phyCORE-MPC5200B-I/O:

Manufacturer	Molex
Number of pins per contact rows	200 (2 rows of 100 pins each)
Molex part number (lead free)	52760-1009 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-MPC5200B-I/O. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3.0 mm) on the underside of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	200 (2 rows of 100 pins each)
Molex part number (lead free)	53467-1009 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	200 (2 rows of 100 pins each)
Molex part number (lead free)	53553-1009 (header)

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

12 Hints for Handling the Module

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!

If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-MPC5200B-I/O into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 6 GND pins that are located right next to the VCC pins must be connected.

13 Real-Time Clock RTC-8564 (U5)

For real-time or time-driven applications, the phyCORE-MPC5200B-I/O is equipped with a RTC-8564 Real-Time Clock at U24. This RTC device provides the following features:

- Serial input/output bus (I²C), address 0xA2
- Power consumption
 - Bus active (400 kHz): < 1 mA
 - Bus inactive, CLKOUT inactive: < 1 μ A
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

The Real-Time Clock is programmed via the I²C bus (address 0xA2 / 0xA3). Since the MPC5200B is equipped with an internal I²C controller, the I²C protocol is processed very effectively without extensive processor action (*refer also to section 0*)

The Real-Time Clock also provides an interrupt output that extends to the /IRQRTC signal X1D33. An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

If the RTC interrupt is to be used as a software interrupt via a corresponding interrupt input of the processor, the signal /IRQRTC must be connected externally with a processor interrupt input.

The RTC_CLKOUT signal can be programmed to various frequencies e.g. 1Hz. The RTC_CLKOUT output must be enabled via solder jumper J12.

For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.

Note:

After connection of the supply voltage the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*).

14 The phyCORE-MPC5200B-I/O on the Carrier Board

PHYTEC Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

14.1 Concept of the Carrier Board phyCORE-MPC5200B-I/O

The Carrier Board phyCORE-MPC5200B-I/O provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MPC5200B-I/O Single Board Computer module. The Carrier Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation. This modular development platform concept is depicted in *Figure 11* and includes the following components:

- The actual **Carrier Board** (1), which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter** (2) and **serial interfaces** (3) of the SBC module at DB-9 connectors (depending on the module, up to two RS-232 interfaces and up to two RS-485 or CAN interfaces).
- All of the signals from the SBC module mounted on the Carrier Board extend to two mating receptacle connectors. A strict 1:1 signal assignment is consequently maintained from the phyCORE-connectors on the module to these expansion connectors. Accordingly, the pin assignment of the **expansion bus** (4) depends entirely on the pinout of the SBC module mounted on the Carrier Board.
-
- As the physical layout of the expansion bus is standardized across all applicable PHYTEC Carrier Boards, we are able to offer various **expansion boards** (5) that attach to the Carrier Board at the expansion bus connectors. These modular expansion boards offer **supplemental I/O functions** (6) as well as peripheral support devices for specific functions offered by the controller populating the **SBC module** (9) mounted on the Carrier Board.
- All controller and on-board signals provided by the SBC module mounted on the Carrier Board are broken out 1:1 to the expansion board by means of its **patch field** (7). The required connections between SBC module / Carrier Board and the expansion board are made using **patch cables** (8) included with the expansion board.

Figure 11 illustrates the modular development platform concept:

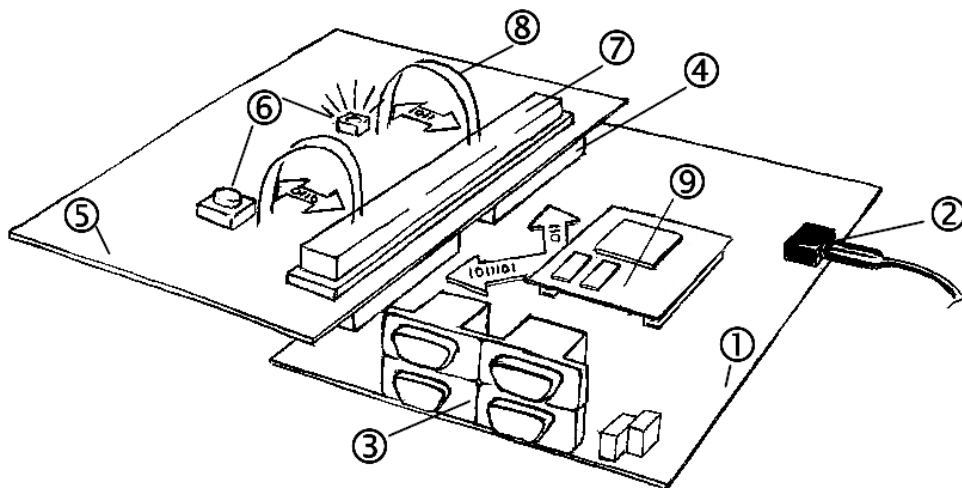


Figure 11: Modular Development and Expansion Board Concept with the phyCORE-MPC5200B-I/O

The following sections contain specific information relevant to the operation of the phyCORE-MPC5200B-I/O mounted on the phyCORE Development MPC5200B-I/O.

14.2 Carrier Board phyCORE-MPC5200B-I/O Connectors and Jumpers

14.2.1 Connectors

As shown in *Figure 12*, the following connectors are available on the phyCORE Development PCM-973:

X1-	phyCORE-connector for phyCORE module with 400 pins (e.g. phyCORE-MPC5200B-I/O)
X2-	phyCORE-connector for phyCORE module with 200 pins (e.g. phyCORE-MPC5200B-tiny)
X3-	400-pin mating receptacle for GPIO expansion board connectivity
X4-	PCI connector for compatible 3.3V PCI insert cards
X5-	JTAG pin header for PCI insert card connector X4
X6-	Connector for supply voltage 9 -14V
X7-	PE connection
X8-	JTAG pin header for FPGA
X9-	JTAG pin header for MPC5200B controller
X10-	Compact Flash card socket
X11-	IDE Interface connector
X12-	FPGA configuration interface
X15-	Base Speaker Interface of the WM9712 (U20)
X16-	Mono out from WM9712
X17-	Beeper out from WM9712
X18-	SPDIF out from WM9712
X19-	Differential output from WM9712
X20-	Auxiliary output from WM9712
P1-	RJ45 Interface for Ethernet connection 10/100MBit
P2-	dual DB-9 plugs for CAN interface connectivity
P3-	dual DB-9 sockets for serial RS232 interface connectivity
P4-	MIC input
P5-	Line in left/right
P6-	Line out left/right
GND1	GND connector for measurement purposes

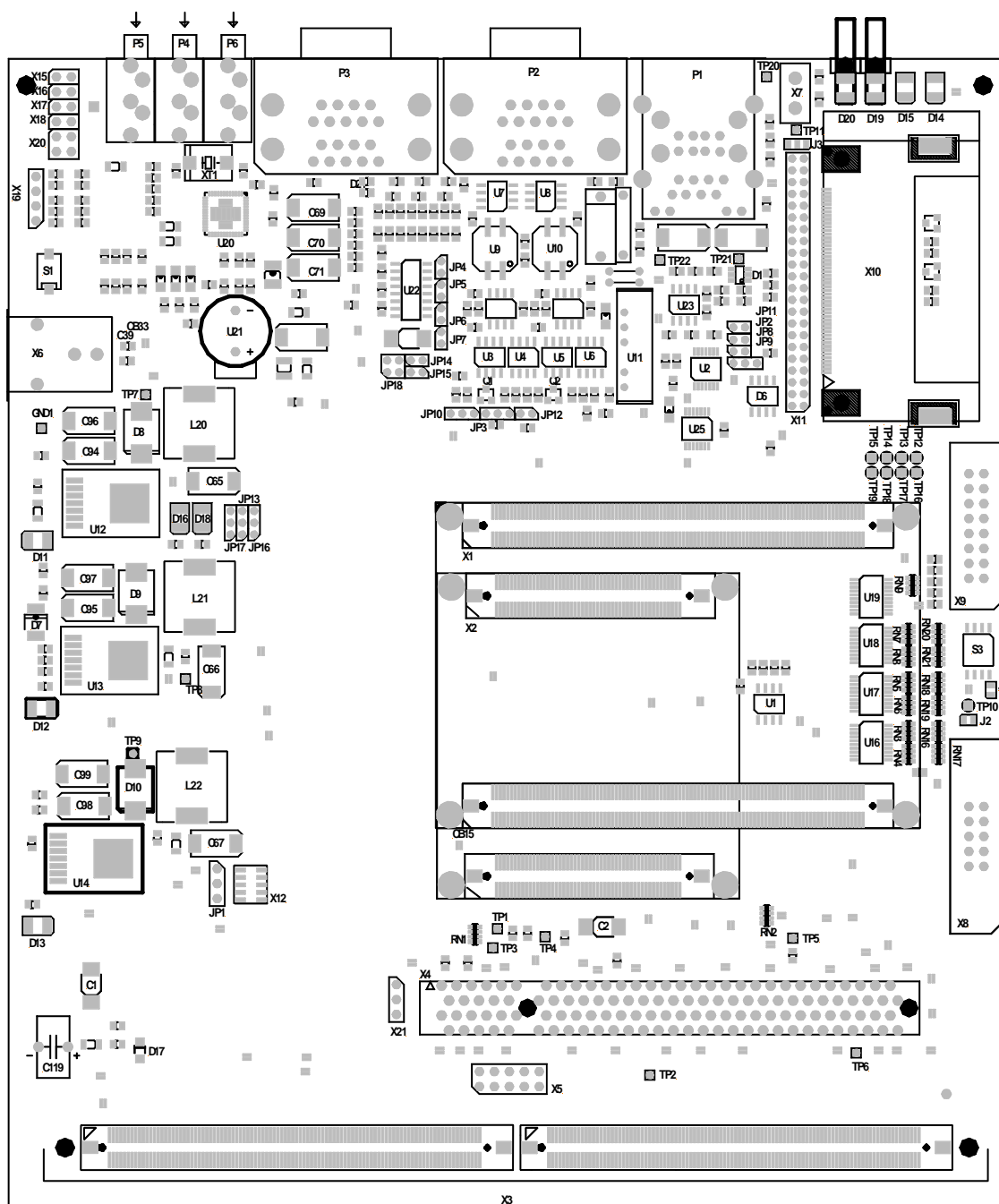


Figure 12: Location of Connectors on the phyCORE-MPC-5200B-I/O Carrier Board

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

14.2.2 Jumpers on the Carrier Board phyCORE-MPC5200B-I/O

Peripheral components of the phyCORE-MPC5200B-I/O Carrier Board can be connected to the signals of the phyCORE-MPC5200B-I/O by setting the applicable jumpers.

The Carrier Board's peripheral components are configured for use with the phyCORE-MPC5200B-I/O by means of removable jumpers. If no jumpers are set, no signals connect to the DB-9 connectors, the control and display units and the CAN transceivers. The Reset input on the phyCORE-

MPC5200B-I/O directly connects to the Reset button (S1).

Figure 13 illustrates the numbering of the jumper pads, while *Figure 14* indicates the location of additional jumpers on the Carrier Board.

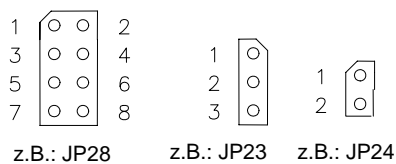


Figure 13: Numbering of Jumper Pads

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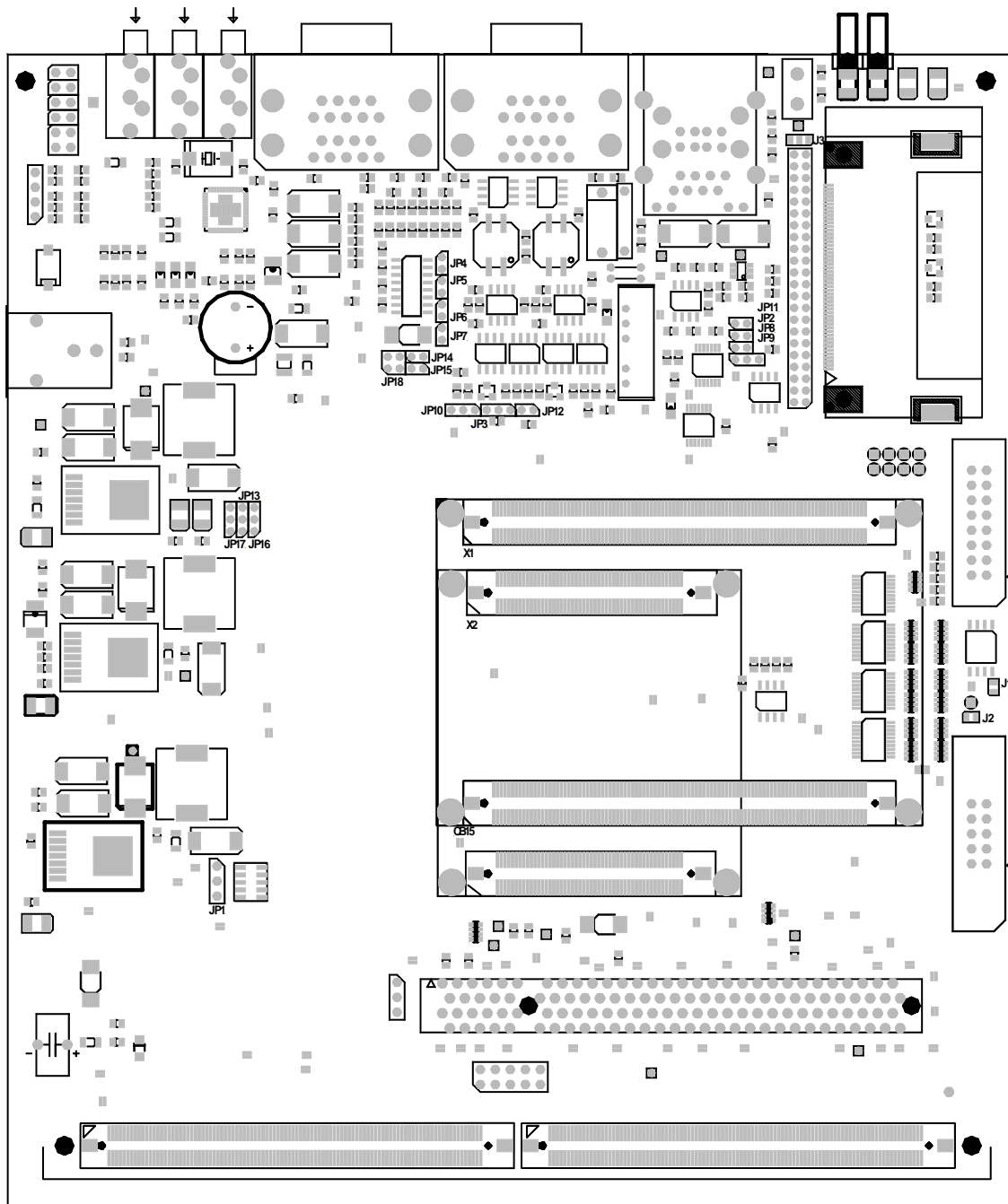


Figure 14: Location of the Jumpers (View of the Component Side)

Figure 15 shows the factory default jumper settings for operation of the phyCORE-MPC5200B-I/O Carrier Board with the standard phyCORE-MPC5200B-I/O (standard = MPC5200B controller, use of first and second RS-232, both CAN interfaces and LED D3 on the Carrier Board). Jumper settings for other functional configurations of the phyCORE-MPC5200B-I/O module mounted on the Carrier Board are described in section 14.3.

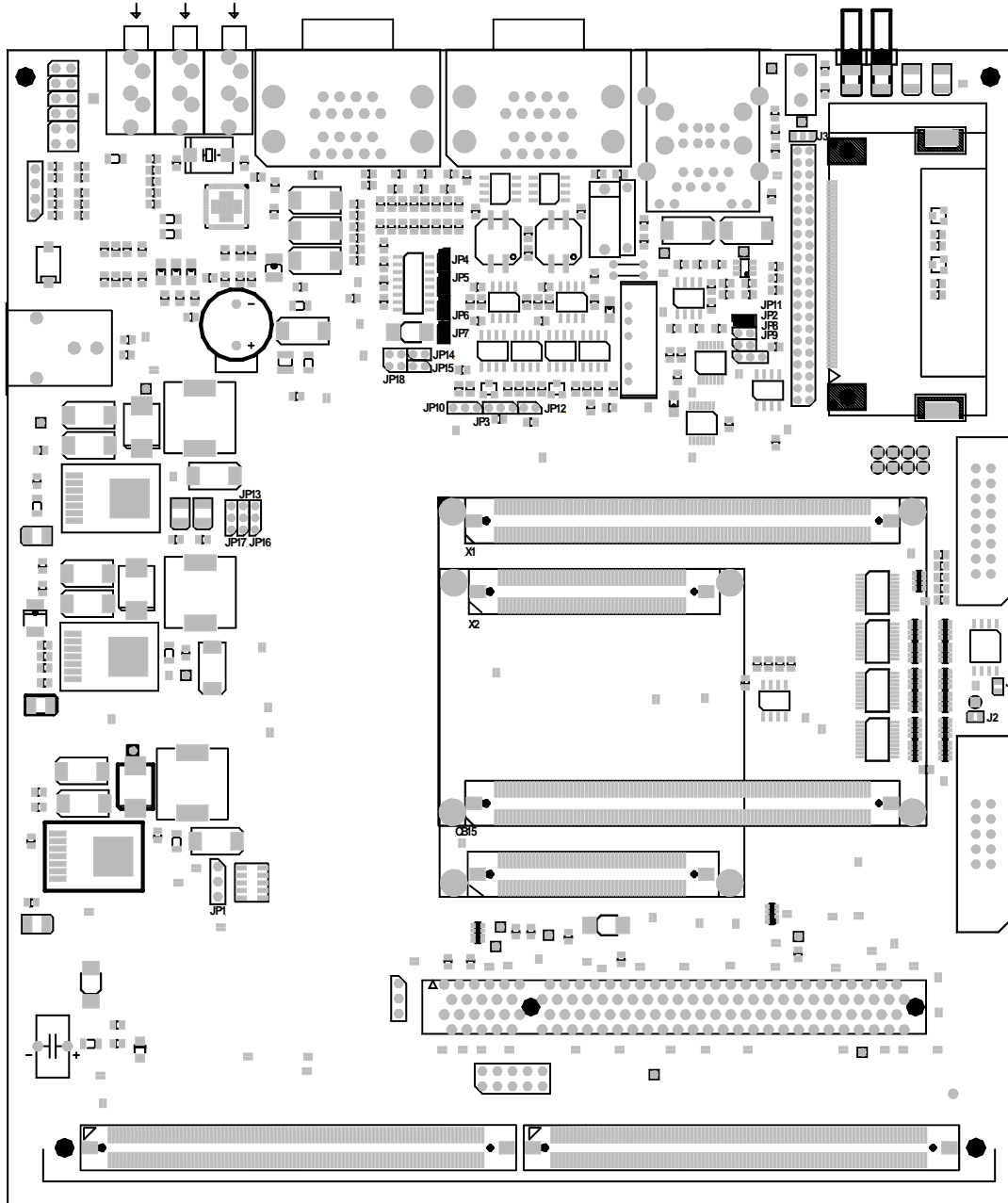


Figure 15: Default Jumper Settings of the phyCORE Development Board MPC5200B-I/O with phyCORE-MPC5200B-I/O

14.3 Functional Components on the phyCORE-MPC5200B-I/O Carrier Board

This section describes the functional components of the phyCORE Carrier Board HD200 supported by the phyCORE-MPC5200B-I/O and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-MPC5200B-I/O module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure 15* and enable alternative or additional functions on the phyCORE-MPC5200B-I/O Carrier Board depending on user needs.

14.3.1 Power Supply at X6

Caution:

Only use the included power adapter to supply power to the Carrier Board! Do not change modules or jumper settings while the Carrier Board is supplied with power!

Permissible input voltage: +/-9 - 14 V DC unregulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-MPC5200B-I/O mounted on the Carrier Board as well as whether an optional expansion board is connected to the Carrier Board. An adapter with a minimum supply of 1.2 A is recommended.

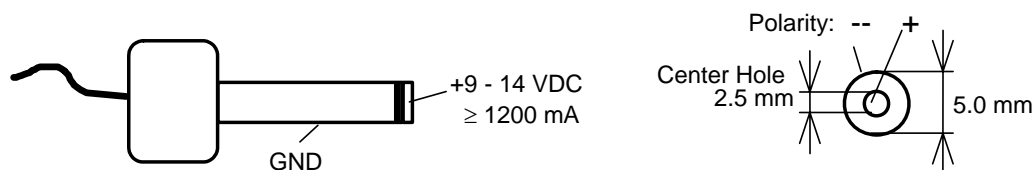


Figure 16: Connecting the Supply Voltage at X6

No jumper configuration is required in order to supply power to the phyCORE-MPC5200B-I/O module!

14.3.2 First Serial Interface at Socket P3A

Socket P3A is the lower socket of the double DB-9 connector at P3. P3A is directly connected to the serial interface PSC3 of the phyCORE-MPC5200B-I/O. The only signal configurable with Jumper JP18 is UART3_CTS_TTL coming from PSC3 on the MPC5200B.

Jumper	Setting	Description
JP18	3 + 4	Signal UART3_CTS_TTL is connected to the RS-232 transceiver U22 on the phyCORE-MPC5200B-I/O Carrier Board, interface signals with RS-232 level are available at connector P3A
JP18	open	UART3_CTS_TTL signal is freely available

Table 14: Jumper Configuration for the First RS-232 Interface

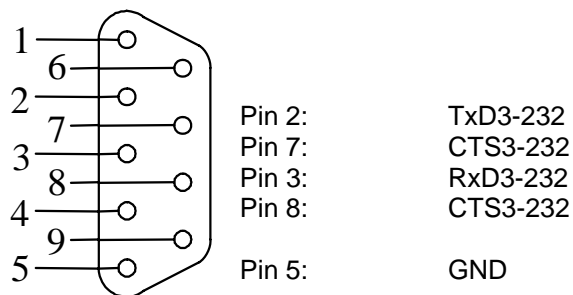


Figure 17: Pin Assignment of the DB-9 Socket P3A as RS-232 (PSC3) (Front View)

14.3.3 Second Serial Interface at Socket P3B

Socket P3B is the upper socket of the double DB-9 connector at P3. P3B is connected directly to the serial interface PSC6 of the phyCORE-MPC5200B-I/O. The only signal configurable with Jumper JP18 is UART6_CTS_TTL coming from PSC6 on the MPC5200B.

Jumper	Setting	Description
JP18	1 + 2	Signal UART6_CTS_TTL is connected to the RS-232 transceiver U22 on the phyCORE-MPC5200B-I/O Carrier Board, interface signals with RS-232 level are available at connector P3B
JP18	open	UART6_CTS_TTL signal is freely available

Table 15: Jumper Configuration of the DB-9 Socket P3B (PSC6)

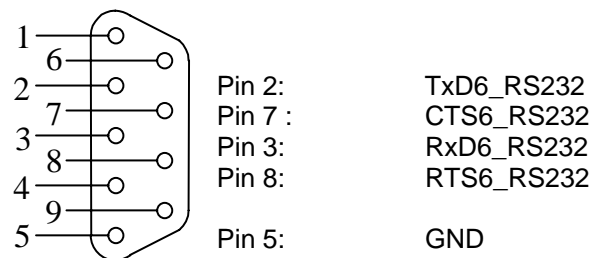


Figure 18: Pin Assignment of the DB-9 Socket P3B as Second RS-232 (Front View)

14.3.4 First CAN Interface at Plug P2A

Plug P2A is the lower plug of the double DB-9 connector at P2. P2A is connected to the first CAN interface (CAN1) of the phyCORE-MPC5200B-I/O via jumpers. There are no CAN transceivers available on the phyCORE-MPC5200B-I/O therefore the transceivers on the Carrier Board must be used. Depending on the configuration of the CAN transceivers and their power supply, the following configuration is possible:

1. CAN signals generated by the Carrier Board CAN transceiver (U9) extend to connector P2A **with galvanic separation**:

Jumper	Setting	Description
JP4	closed	Input at opto-coupler U3 on the Carrier Board connected to CAN1_TX signal from the phyCORE-MPC5200B-I/O
JP5	closed	Output at opto-coupler U4 on the Carrier Board connected to CAN1_RX signal of the phyCORE-MPC5200B-I/O

Table 16: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Carrier Board

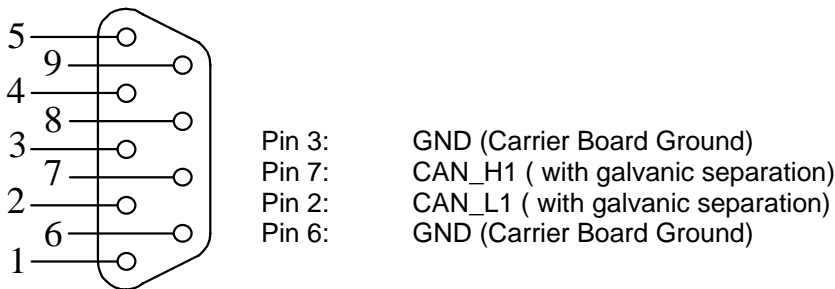


Figure 19: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Carrier Board)

Caution:

When using the DB-9 connector P2A as CAN interface and the CAN transceiver on the Carrier Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP4	open	CAN1_TX signal not connected to transceiver, no CAN communication possible
JP5	open	CAN1_RX signal not connected to transceiver, no CAN communication possible

Table 17: Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on the Carrier Board)

14.3.5 Second CAN Interface at Plug P2B

Plug P2B is the upper plug of the double DB-9 connector at P2. P2B is connected to the second CAN interface (CAN2) of the phyCORE-MPC5200B-I/O via jumpers. There are no CAN transceivers available on the phyCORE-MPC5200B-I/O therefore the transceivers on the Carrier Board must be used. Depending on the configuration of the CAN transceivers and their power supply, the following configuration is possible:

1. CAN signals generated by the Carrier Board CAN transceiver (U10) extend to connector P2B **with galvanic separation:**

Jumper	Setting	Description
JP6	closed	Input at opto-coupler U5 on the Carrier Board connected to CAN2_TX signal from the phyCORE-MPC5200B-I/O
JP7	closed	Output at opto-coupler U6 on the Carrier Board connected to CAN2_RX signal of the phyCORE-MPC5200B-I/O

Table 18: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Carrier Board HD200

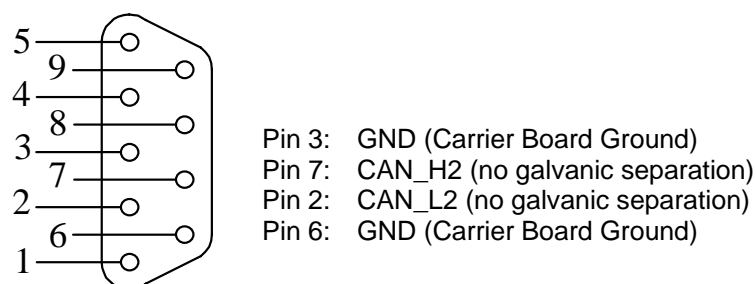


Figure 20: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Carrier Board)

Caution:

When using the DB-9 connector P2B as second CAN interface and the CAN transceiver on the Carrier Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP6	open	CAN2_TX signal not connected to transceiver, no CAN communication possible
JP7	open	CAN2_RX signal not connected to transceiver, no CAN communication possible

Table 19: Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on the Carrier Board)

14.3.6 Programmable LED D16

The phyCORE Carrier Board MPC5200B offers a programmable LED at D16 for user implementations. This LED can be connected to port pin Gpio_Wkup_7 (ball C12) or to the SPI_MOSI signal (ball B5) of the MPC5200B CPU. A low-level at applicable port pin causes the LED to illuminate, LED D16 remains off when writing a high-level.

Jumper	Setting	Description
JP13	1 + 2	Port pin SPI_MOSI of the MPC5200B controls LED D16 on the Carrier Board
JP13	2 + 3	Port pin Gpio_Wkup_7 of the MPC5200B controls LED D16 on the Carrier Board

Table 20: JP17 Configuration of the Programmable LED D3

14.3.7 Ethernet Interface P1A

The Ethernet interface of the phyCORE-MPC5200B-I/O is accessible at an RJ45 connector (P1A) on the Carrier Board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK and SPEED indication are integrated in the connector. Two additional LEDs at D19 and D20 are provided to allow display of other Ethernet transmission states. These LEDs can be used to indicate transmission type and possible collisions that may occur on the Ethernet network. Jumpers JP8 and JP9 allow configuration of additional Ethernet PHY interface signals. The following configuration options are possible:

Jumper	Setting	Description
JP8	open	/ETH_INT from PHY on the phyCORE-MPC5200B-I/O not connected
	closed	/ETH_INT from PHY on the phyCORE-MPC5200B-I/O connected to /IRQ1 on the phyCORE module
JP9	open	PHY transceiver /ETH_PD input on the phyCORE-MPC5200B-I/O not connected
	1 + 2	PHY transceiver /ETH_PD input on the phyCORE-MPC5200B-I/O connected to SPI_MISO signal on the phyCORE module
	2 + 3	PHY transceiver /ETH_PD input on the phyCORE-MPC5200B-I/O connected to GPIO7 signal on the phyCORE module

Table 21: JP8, JP9 Ethernet Interface Configuration

14.3.8 USB Host Interface P1B

The USB Host interface of the phyCORE-MPC5200B-I/O is accessible at connector P1B on the Carrier Board. This interface is compliant with USB version 1.1 and its mode can be configured with the help of Jumper JP2. The following configuration options are possible:

Jumper	Setting	Description
JP2	open	VMO mode selected
	closed	FSEO mode selected

Table 22: JP2 USB Host Interface Configuration

A second USB connector is provided at P1C. However, this connector does not carry any USB communication signals. Connector P1C can only be used to access the USB supply voltage.

14.3.9 Audio Interface

The AC97 interface on the phyCORE-MPC5200B-I/O connects to a Wolfson WM9712 audio codec controller on the Carrier Board. A variety of signals generated by the WM9712 IC are available at the following connectors:

- Header X15 - Base Speaker
- Header X18 - SPDIF OUT
- Header X19 - Differential Output
- Header X20 - Auxiliary Output
- Socket P4 - MIC1/MIC2
- Socket P5 - LINE IN R/L
- Socket P6 - LINE OUT R/L

Jumpers JP14 and JP15 are available for configuration of interrupt signals generated by the WM9712 device. The following configuration options are possible:

Jumper	Setting	Description
JP14	open	AC_INT signal on WM9712 not used
	closed	AC_INT signal connected to /IRQ_2 on the phyCORE-MPC5200B-I/O
JP15	open	PEN_INT signal from WM9712 not used
	closed	PEN_INT signal connected to /IRQ_3 on the phyCORE-MPC5200B-I/O

Table 23: JP14, JP15 AC97 Audio Interface Configuration

14.3.10 Compact Flash Card Socket X10

The phyCORE-MPC5200B-I/O Carrier Board provides a Compact Flash (CF) card socket at X10. CF cards used in this socket can only be operated in IDE mode. Activity on the CF card socket is indicated by LED D14. Jumpers J3 and JP11 are available for configuration of the Compact Flash card interface. The following configuration options are possible:

Jumper	Setting	Description
J3	open	<i>Not recommended!</i>
	1 + 2	Compact Flash card write protection active
	2 + 3	Compact Flash card write protection not active
JP11	open	Compact Flash slave mode selected
	closed	Compact Flash master mode selected

Table 24: J3, JP11 CF Card Interface Configuration

14.3.11 IDE Interface X11

The phyCORE-MPC5200B-I/O Carrier Board provides an IDE interface header at X11 for connection to external 2.5" hard disks. The 44-pin header connector in 2.0 mm pin spacing allows easy and convenient connection to peripheral devices using a ribbon cable. Activity on the IDE socket is indicated by LED D15.

14.3.12 PCI Card Slot X4

The phyCORE-MPC5200B-I/O Carrier Board provides a 3.3V PCI interface connector at X4. All common 3.3V PCI insert cards can be used in this slot allowing the user to add additional interface features to this hardware platform. Configuration of the PCI interface via jumpers is not necessary. Only the required interrupt sources can be configured via SMD resistors. Resistors R95-R98 on the Carrier Board connect the available interrupts. Only R95 is placed as the default configuration connecting /PCI_INTA with /IRQ_0. Additional interrupt sources can be made available by adding the corresponding resistor on the Carrier Board.

Note:

The current draw of the PCI application in combination with the power consumption of all other circuitry used at the same time must not exceed the allowed maximum current draw for the phyCORE-MPC5200B-I/O and Carrier Board hardware combination.

14.3.13 Misc. Configuration Jumpers on the Carrier Board

The following table describes additional jumpers provided for configuration of the Carrier Board or the phyCORE-MPC5200B-I/O operated on it:

Jumper	Setting	Description
JP3	open	Default Boot configuration of the connected phyCORE-MPC5200B-I/O will be used
	1 + 2	Boot configuration of the inserted phyCORE-MPC5200B-I/O will be overwritten by a LOW level
	2 + 3	Boot configuration of the inserted phyCORE-MPC5200B-I/O will be overwritten by a HIGH level
JP10	open	Default Flash Bank Select configuration of the connected phyCORE-MPC5200B-I/O will be used
	1 + 2	Flash Bank Select configuration of the inserted phyCORE-MPC5200B-I/O will be overwritten by a LOW level
	2 + 3	Flash Bank Select configuration of the inserted phyCORE-MPC5200B-I/O will be overwritten by a HIGH level
JP12	open	Independent JTAG clocks for FPGA JTAG interface Controller JTAG interface
	closed	JTAG clock for controller and FPAG connected (only applicable in conjunction with corresponding settings at DIP switch S3 generating a Boundary Scan chain)

Table 25: Misc. Configuration Jumpers JP3, JP10, JP12

14.3.14 FPGA JTAG Connector X8

Connector X8 provide access to the JTAG signals for the FPGA on the phyCORE-MPC5200B-I/O module:

Signal	Pin#	Pin#	Signal
FPGA_TCK	1	2	GND
FPGA_TDO	3	4	3.3V
FPGA_TMS	5	6	n.c. (default), J1 connects to 3.3V
n.c.	7	8	n.c.
FPGA_TDI	9	10	GND

Table 26: FPGA JTAG Connector X8 Pin Assignment

14.3.15 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

As described in *section 14.1*, all signals from the phyCORE-MPC5200B-I/O extend in a strict 1:1 assignment to the Expansion Bus connector X3 on the Carrier Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Carrier Board at X3.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the Expansion Bus connector (X3 on the Carrier Board) as well as the patch field.

However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

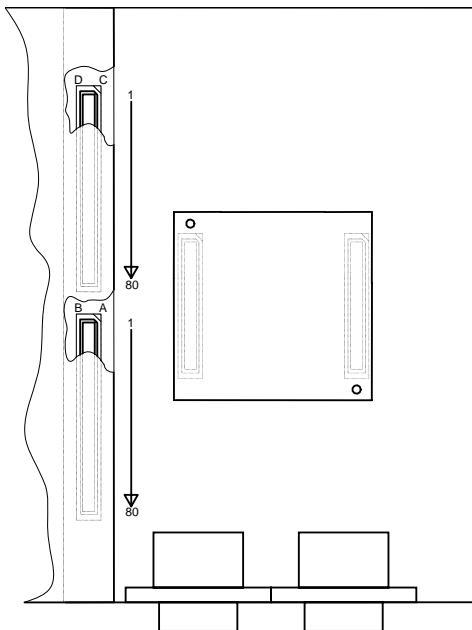


Figure 21: Pin Assignment Scheme of the Expansion Bus

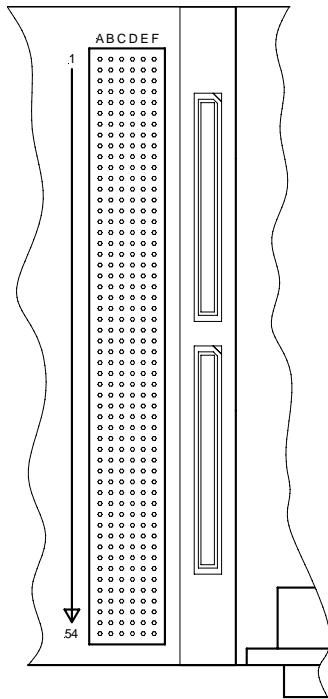


Figure 22: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-MPC5200B-I/O, in conjunction with the Expansion Bus (X3) on the Carrier Board and the patch field on an expansion board, is as follows:

Signal	phyCORE Module	Expansion Bus	Patch Field
Ext_AD0	100B	99A	X15-25
Ext_AD1	100A	98B	X13-25
Ext_AD2	99A	98A	X14-25
Ext_AD3	98B	97B	X12-25
Ext_AD4	98A	96A	X17-24
Ext_AD5	97B	96B	X11-25
Ext_AD6	96B	95A	X16-24
Ext_AD7	96A	95B	X10-25
Ext_AD8	95A	93B	X13-24
Ext_AD9	94A	93A	X14-24
Ext_AD10	93B	91B	X11-24
Ext_AD11	93A	91A	X17-22
Ext_AD12	92B	90B	X10-24
Ext_AD13	91B	90A	X16-22
Ext_AD14	91A	88B	X13-22
Ext_AD15	90B	89A	X15-22
Ext_AD16	83B	83A	X14-21
Ext_AD17	83A	78B	X13-20
Ext_AD18	82B	81A	X17-20
Ext_AD19	81B	77B	X12-20
Ext_AD20	81A	80A	X16-20
Ext_AD21	80B	76B	X11-20
Ext_AD22	80A	79A	X15-20
Ext_AD23	79A	75B	X10-20
Ext_AD24	77B	78A	X14-20
Ext_AD25	76B	72B	X12-19
Ext_AD26	76A	75A	X16-19
Ext_AD27	75B	71B	X11-19
Ext_AD28	75A	74A	X15-19
Ext_AD29	74A	70B	X10-19
Ext_AD30	73B	73A	X14-19
Ext_AD31	73A	68B	X13-17

Table 27: Pin Assignment Data/Address Bus for the phyCORE-MPC5200B-I/O / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/LP_CS1	5A	5A	X16-1
/LP_CS2	35B	35B	X10-10
/LP_CS3	5B	5B	X10-2
/LP_Cs4	6B	6B	X11-2
/LP_Cs5	36B	36B	X11-10
/LP_Cs6	47B	47B	X12-12
/LP_Cs7	48B	48B	X13-12
/LP_Ts	33B	33B	X13-9
LP_Ack	34A	34A	X15-9
/LP_Ale	6A	6A	X17-1
/LP_Oe	8A	8A	X14-2
LP_RD/WR	7B	7B	X12-2

Table 28: Pin Assignment Dedicated LocalPlus Control Signals
phyCORE-MPC5200B-I/O / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/Pci_Reset	70A	70A	X16-17
Pci_Clock	70B	66B	X11-17
/Pci_Gnt	71A	71A	X17-17
/Pci_Req	72B	67B	X12-17
/Pci_Cbe_3	78A	73B	X13-19
Pci_Idsel	78B	76A	X17-19
/Pci_Cbe_2	84A	80B	X10-21
/Pci_Irdy	85A	81B	X11-21
/Pci_Frame	85B	84A	X15-21
/Pci_Devsel	86A	82B	X12-21
/Pci_Trdy	86B	85A	X16-21
/Pci_Stop	87B	86A	X17-21
/Pci_Perr	88A	85B	X10-22
Pci_Par	88B	88A	X14-22
/Pci_Serr	89A	86B	X11-22
/Pci_Cbe_1	90A	87B	X12-22
/Pci_Cbe_0	95B	94A	X15-24

Table 29: Pin Assignment PCI dedicated signals
phyCORE-MPC5200B-I/O / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
ATA_Isolation	67B	61B	X11-16
/ATA_lor	68A	65A	X16-16
/ATA_Dack	68B	62B	X12-16
ATA_intrq	69A	66A	X17-16
ATA_Cs1	65A	63A	X14-16
ATA_Drq	65B	58B	X13-15
ATA_Cs0	64A	61A	X17-15
ATA_lochrdy	66A	64A	X15-16
/ATA_low	66B	60B	X10-16

Table 30: Pin Assignment Dedicated ATA /IDE Interface Signals
phyCORE-MPC5200B-I/O / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
AC97_1_Sdata_In	16C	-	-
AC97_1_Sdata_O	15D	-	-
AC97_1_Res	13C	-	-
AC97_1_Sync	14C	-	-
AC97_1_Bitclk	15C	-	-
TXD6-232	23C	23C	X5-6
RXD6-232	21C	21C	X2-6
UART6_TXD_TTL	20C	20C	X8-5
UART6_RXD_TTL	19C	19C	X7-5
UART6_RTS_TTL	24C	24C	X7-6
UART6_CTS_TTL	25C	25C	X8-6
RXD3-232	22D	22D	X4-6
TXD3-232	23D	23D	X6-6
UART3_TXD_TTL	17D	17D	X4-5
UART3_RXD_TTL	16D	16D	X3-5
UART3_RTS_TTL	25D	25D	X9-6
UART3_CTS_TTL	26D	26D	X3-7
CAN1_TX	21D	21D	X3-6
CAN1_RX	20D	20D	X9-5
CAN2_TX	18C	18C	X5-5
CAN2_RX	18D	18D	X6-5
I2C1_Clk	31C	31C	X2-9
I2C1_Io	32D	32D	X4-9
I2C2_Clk	26C	26C	X2-7
I2C2_Io	28C	28C	X5-7
SPI_Mosi	27D	27D	X4-7
SPI_Miso	28D	28D	X6-7
SPI_Clk	30D	30D	X9-7
SPI_Ss	31D	31D	X3-9
ETH_RX-	35C	-	-
ETH_RX+	35D	-	-
ETH_TX-	36C	-	-
ETH_TX+	36D	-	-
/ETH_INT	37D	-	-
ETH_LINK	33C	-	-
ETH_SPEED	34C	-	-
/ETH_PD	38C	-	-
USB1_Oe	50C	-	-
USB1_TXP	48D	-	-
USB1_TXN	49C	-	-
USB1_RXD	46D	-	-
USB1_RXP	47D	-	-
USB1_RXN	48C	-	-
USB1_Suspend	46C	-	-
USB1_PortPwr	43D	-	-
USB1_Overcnt	45C	-	-
USB1_Speed	45D	-	-

Table 31: Pin Assignment Interfaces for the phyCORE-MPC5200B-I/O / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
CPU_TCK	38D	-	-
/COP_TRST	39C	-	-
CPU_TDI	40D	-	-
CPU_TDO	41D	-	-
CPU_TMS	42D	-	-
CK_STOP	40C	-	-
/CPU_TRST	41C	-	-

Table 32: Pin Assignment COP Interface Signals for the
phyCORE-MPC5200B-I/O /Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/IRQ_0	4A	4A	X15-1
/IRQ_1	2B	2B	X12-1
/IRQ_2	3B	3B	X13-1
/IRQ_3	3A	3A	X14-1
Timer2	12D	12D	X4-4
Timer3	13D	13D	X6-4
Timer4	61C	61C	X2-16
Timer5	44C	44C	X7-11
Timer6	60C	60C	X8-15
Timer7	36A	36A	X17-9
/RESIN	10D	10D	X2-4
/HReset	11C	11C	X9-2
/SReset	10C	10C	X9-1
/PWR_GOOD	7D	7D	X7-1
/FL_WP	9C	9C	X8-2
GPIO7	11D	11D	X3-4
RTC_CLKOUT	1B	1B	X11-1
/IRQRTC	33D	33D	X6-9
PSC2_4	43C	43C	X5-11
ETH_TXD3	58D	58D	X6-15
ETH_TXD2	59C	59C	X7-15
ETH_TXD1	60D	60D	X9-15
ETH_TXD0	61D	61D	X3-16
ETH_RXD3	51C	51C	X2-14
ETH_RXD2	52D	52D	X4-14
ETH_RXD1	53C	53C	X5-14
ETH_RXD0	54C	54C	X7-14
ETH_CRS	50D	50D	X9-12
ETH_RXERR	51D	51D	X3-14
ETH_TXCLK	53D	53D	X6-14
ETH_RXCLK	55D	55D	X9-14
ETH_MDIO	56D	56D	X3-15
ETH_MDC	57D	57D	X4-15
ETH_TXEN	62D	62D	X4-16
ETH_TXERR	58C	58C	X5-15
ETH_RXDV	56C	56C	X2-15
ETH_COL	55C	55C	X8-14
Test_Sel_1	35A	35A	X16-9
ETH_NWAYEN	30C	30C	X8-7
ETH_DUPLEX	29C	29C	X7-7
WDI	8D	8D	X7-2
/WDO	8C	8C	X8-1

Table 33: Pin Assignment Misc. Control Signals for the
phyCORE-MPC5200B-I/O /Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
FPGA_TDO	61A	-	-
FPGA_TMS	62B	-	-
FPGA_TDI	63A	-	-
FPGA_TCK	63B	-	-
FPGA_B1_C1	31B	31B	X11-9
FPGA_B1_C2	32B	32B	X12-9
FPGA_B1_D1	33A	33A	X14-9
FPGA_B1_D2	37B	37B	X12-10
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FPGA_B1_L2	53A	53A	X14-14
FPGA_B1_L3	53B	53B	X13-14
FPGA_B1_L4	54A	54A	X15-14
FPGA_B1_M1	55A	55A	X16-14
FPGA_B1_M2	55B	55B	X10-15
FPGA_B1_M3	56A	56A	X17-14
FPGA_B1_M4	56B	56B	X11-15
FPGA_B1_N1	57B	57B	X12-15
FPGA_B1_N2	58A	58A	X14-15
FPGA_B1_N3	58B	33C	X5-9
FPGA_B1_N4	59A	59A	X15-15
FPGA_B1_P1	60A	60A	X16-15
FPGA_B1_P2	60B	34C	X7-9
FPGA_B1_P3	61B	35D	X9-9
FPGA_B2_C11	8B	8B	X13-2
FPGA_B2_D8	9A	9A	X15-2
FPGA_B2_G11	10A	10A	X16-2
FPGA_B2_F10	10B	10B	X10-4
FPGA_B2_G10	11A	11A	X17-2
FPGA_B2_F9	11B	11B	X11-4

Signal	phyCORE Module	Expansion Bus	Patch Field
FPGA_B2_D11	12B	12B	X12-4
FPGA_B2_B11	13A	13A	X14-4
FPGA_B2_D10	13B	13B	X13-4
FPGA_B2_A11	14A	14A	X15-4
FPGA_B2_B9	15A	15A	X16-4
FPGA_B2_B10	15B	15B	X10-5
FPGA_B2_A9	16A	16A	X17-4
FPGA_B2_A10	16B	16B	X11-5
FPGA_B2_B8	17B	17B	X12-5
FPGA_B2_F8	18A	18A	X14-5
FPGA_B2_A8	18B	18B	X13-5
FPGA_B2_F7	19A	19A	X15-5
FPGA_B2_A7	20A	20A	X16-5
FPGA_B2_G7	20B	20B	X10-6
FPGA_B2_B7	21A	21A	X17-5
FPGA_B2_G6	21B	21B	X11-6
FPGA_B2_F6	22B	22B	X12-6
FPGA_B2_D6	23A	23A	X14-6
FPGA_B2_E6	23B	23B	X13-6
FPGA_B2_C6	24A	24A	X15-6
FPGA_B2_A6	25A	25A	X16-6
FPGA_B2_C5	25B	25B	X10-7
FPGA_B2_B6	26A	26A	X17-6
FPGA_B2_C4	26B	26B	X11-7
FPGA_B2_A5	27B	27B	X12-7
FPGA_B2_A4	28A	28A	X14-7
FPGA_B2_B5	28B	28B	X13-7
FPGA_B2_B4	29A	29A	X15-7
FPGA_B2_A3	30A	30A	X16-7
FPGA_B2_D9	30B	30B	X10-9
FPGA_B2_B3	31A	31A	X17-7
FPGA_B2_A12	63C	63C	X5-16
FPGA_B2_B12	64C	64C	X7-16
FPGA_B2_A14	65C	65C	X8-16
FPGA_B2_C12	65D	65D	X9-16
FPGA_B2_B14	66C	66C	X2-17
FPGA_B2_C13	66D	66D	X3-17
FPGA_B2_A13	67D	67D	X4-17
FPGA_B2_B13	68D	68D	X6-17
FPGA_B2_D7	68C	68C	X5-17
FPGA_B3_C14	69C	69C	X7-17
FPGA_B3_C15	70C	70C	X8-17
FPGA_B3_C16	70D	70D	X9-17
FPGA_B3_D13	71C	71C	X2-19
FPGA_B3_D14	71D	71D	X3-19
FPGA_B3_D15	72D	72D	X4-19
FPGA_B3_D16	73C	73C	X5-19
FPGA_B3_E13	73D	73D	X6-19
FPGA_B3_E14	74C	74C	X7-19
FPGA_B3_E15	75C	75C	X8-19

Signal	phyCORE Module	Expansion Bus	Patch Field
FPGA_B3_E16	75D	75D	X9-19
FPGA_B3_F13	76C	76C	X2-20
FPGA_B3_F14	76D	76D	X3-20
FPGA_B3_F15	77D	77D	X4-20
FPGA_B3_F16	78C	78C	X5-20
FPGA_B3_G12	78D	78D	X6-20
FPGA_B3_G13	79C	79C	X7-20
FPGA_B3_G15	80C	80C	X8-20
FPGA_B3_G16	80D	80D	X9-20
FPGA_B3_H11	81C	81C	X2-21
FPGA_B3_H12	81D	81D	X3-21
FPGA_B3_H13	82D	82D	X4-21
FPGA_B3_H15	83C	83C	X5-21
FPGA_B3_J11	83D	83D	X6-21
FPGA_B3_J12	84C	84C	X7-21
FPGA_B3_J15	85C	85C	X8-21
FPGA_B3_J16	85D	85D	X9-21
FPGA_B3_K13	86C	86C	X2-22
FPGA_B3_K15	86D	86D	X3-22
FPGA_B3_K16	87D	87D	X4-22
FPGA_B3_L12	88C	88C	X5-22
FPGA_B3_L14	88D	88D	X6-22
FPGA_B3_L15	89C	89C	X7-22
FPGA_B3_L16	90C	90C	X8-22
FPGA_B3_M12	90D	90D	X9-22
FPGA_B3_M14	91C	91C	X2-24
FPGA_B3_M15	91D	91D	X3-24
FPGA_B3_M16	92D	92D	X4-24
FPGA_B3_N12	93C	93C	X5-24
FPGA_B3_N15	93D	93D	X6-24
FPGA_B3_N16	94C	94C	X7-24
FPGA_B3_P14	95C	95C	X8-24
FPGA_B3_P15	95D	95D	X9-24
FPGA_B3_P16	96C	96C	X2-25
FPGA_B4_K6	96D	96D	X3-25
FPGA_B4_K7	97D	97D	X4-25
FPGA_B4_N6	98C	98C	X5-25
FPGA_B4_N7	98D	98D	X6-25
FPGA_B4_P6	99C	99C	X7-25
FPGA_B4_R6	100C	100C	X8-25

Table 34: Pin Assignment FPGA Signals for the phyCORE-MPC5200B-I/O /Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
3V3_PCI	-	1C, 2C, 1D, 2D	X2-1, X2-2, X3-1, X3-2
3V3	1C, 2C, 4C, 5C, 1D, 2D	4C, 5C	X4-1, X4-2
FGPA_VCCIO	4D, 5D	4D, 5D über Jumper	X5-1, X5-2
VCC_SRAM	6D	6D	X6-2
VBAT	6C	6C	X6-1
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 71B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	X2-3, X2-8, X2-13, X2-18, X2-23 X3-3, X3-8, X3-13, X3-18, X3-23 X4-3, X4-8, X4-13, X4-18, X4-23 X5-3, X5-8, X5-13, X5-18, X5-23 X6-3, X6-8, X6-13, X6-18, X6-23 X7-3, X7-8, X7-13, X7-18, X7-23 X8-3, X8-8, X8-13, X8-18, X8-23 X9-3, X9-8, X9-13, X9-18, X9-23, X10-3, X10-8, X10-13, X10-18, X10-23 X11-3, X11-8, X11-13, X11-18, X11-23 X12-3, X12-8, X12-13, X12-18, X12-23 X13-3, X13-8, X13-13, X13-18, X13-23 X14-3, X14-8, X14-13, X14-18, X14-23 X15-3, X15-8, X15-13, X15-18, X15-23 X16-3, X16-8, X16-13, X16-18, X16-23 X17-3, X17-8, X17-13, X17-18, X17-23,

Table 35: Pin Assignment Power Supply for the phyCORE-MPC5200B-I/O / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
N.C.	1A, 100D	15C, 16C, 35C, 36C, 38C, 39C, 40C, 45C, 46C, 48C, 49C, 50C, 36D, 37D, 38D, 40D, 41D, 42D, 43D, 45D, 46D, 47D, 48D, 100D	X8-4, X2-5, X8-9, X2-10, X5-10, X7-10, X8-10, X8-11, X2-12, X5-12, X7-12, X8-12, X3-10, X4-10, X6-10, X9-10, X3-11, X4-11, X6-11, X9-11, X3-12, X4-12, X6-12, X9-25

Table 36: Unused Pins on the phyCORE-MPC5200B-I/O / Carrier Board / Expansion Board

14.3.16 Gold CAP Connector C119

The mounting space C119 (see *PCB stencil*) is provided for connection of a gold cap that buffers the RTC and the SRAM on the phyCORE-MPC5200B-I/O. In the event of a VCC operating voltage failure the RTC and SRAM is automatically supplied with power from the connected gold cap. The optional gold cap required for the RTC and SRAM buffering is available through PHYTEC (order code CG-002).

15 Revision History

Date	Version numbers	Changes in this manual
7-Mar-2007	Manual L694e_0 PCM-032 PCB# 1250.1 PCM-973 PCB# 1260.0	First draft, Preliminary documentation. phyCORE-MPC5200B-I/O in "Prototype" state

16 Component Placement Diagram

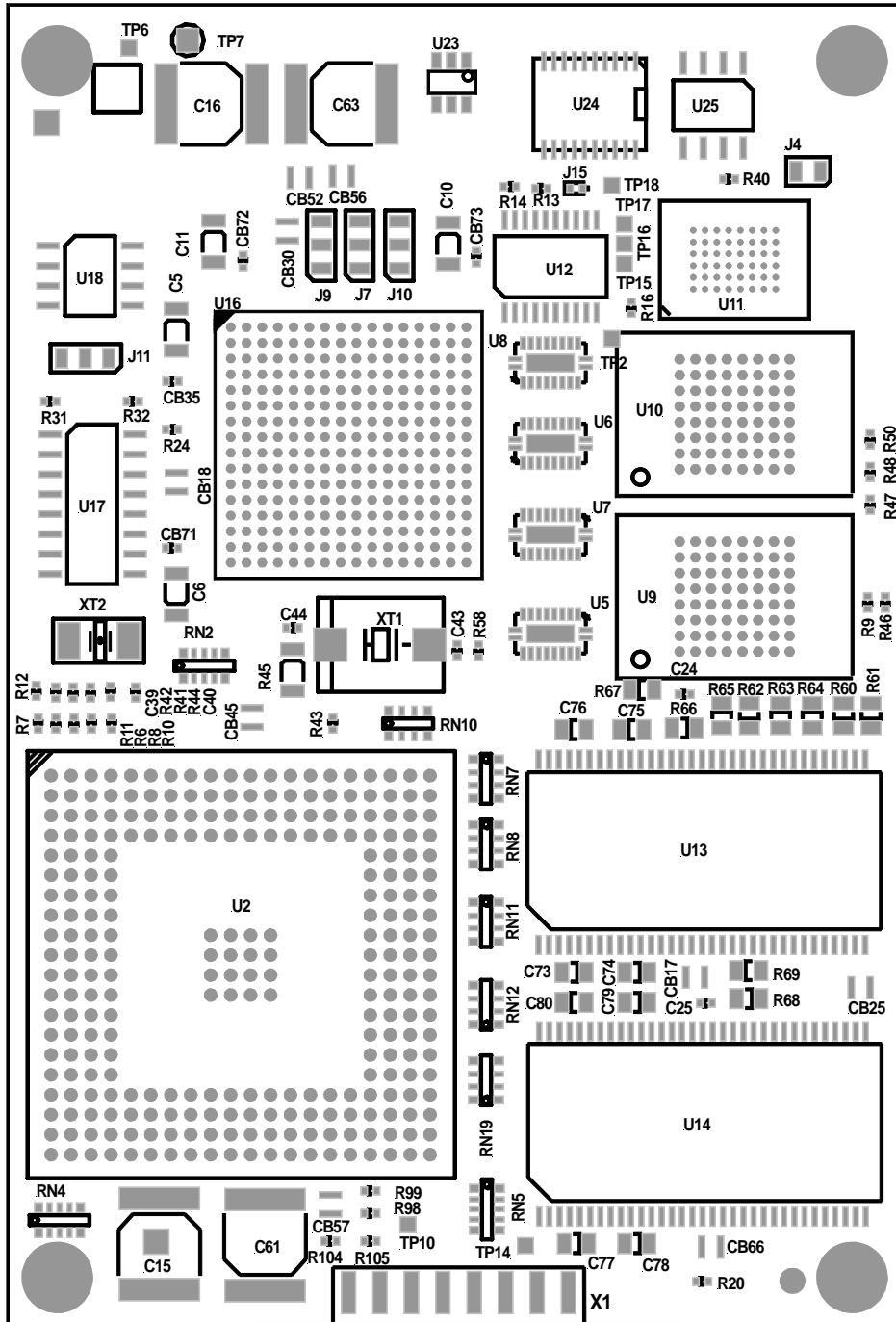


Figure 23: phyCORE-MPC5200B-I/O Component Placement, Top View

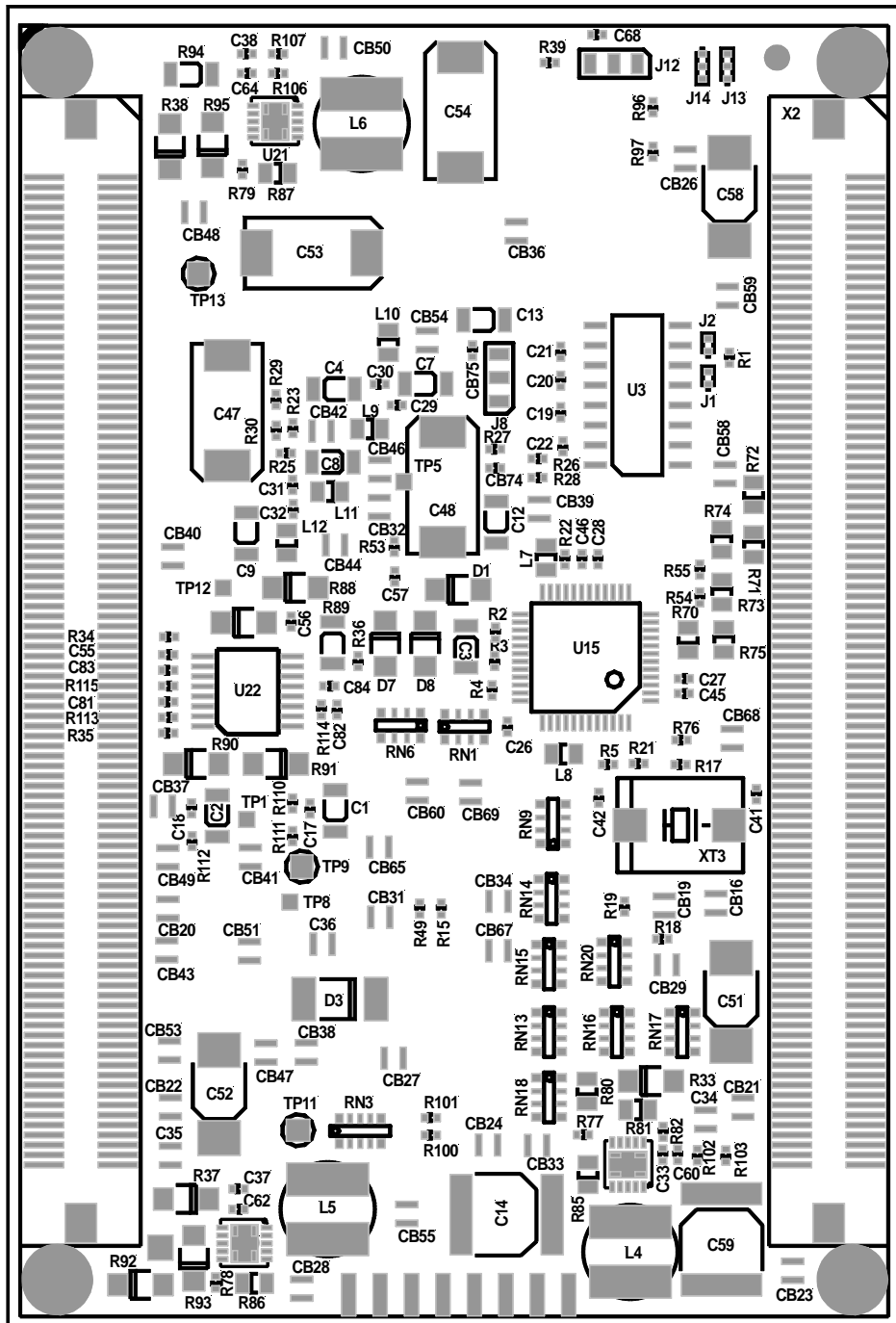


Figure 24: phyCORE-MPC5200B-I/O Component Placement, Bottom View

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A Appendix

A.1 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Document:	phyCORE-MPC5200B-I/O
Document number:	L-694e_1, Edition, April 2008

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