phyCORE-ETH16

Hardware Manual

Edition March 2002

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	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 255 Ericksen Avenue NE Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 info@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

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Preface

This phyCORE-ETH16 Hardware Manual describes the board's design and functions. Precise specifications for the CS8900A Ethernet controller can be found in the enclosed CS8900A Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity for the PHYTEC phyCORE-ETH16

PHYTEC Single Board Computers and Add-on Boards (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by Electro Static Discharge (ESD) and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-ETH16 Adapter is one of a series of PHYTEC Add-on boards supporting our Single Board Computers (SBCs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional micro- / mini- and phyCORE OEM modules which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The adapter supports the Ethernet standard according to IEEE802.3 and has a transfer rate of 10 Mbit/s. The Ethernet connection is established over an RJ45 connector. This manual contains descriptions of configuration options and the pin layout of the phyCORE-ETH16.

The CS8900A from CIRRUS LOGIC is integrated as an Ethernet controller. A 1 kBit serial EEPROM is available for storage of the following setup information:

- Ethernet Individual Address (MAC address)
- I/O base address
- Interrupt number

The Ethernet controller CS8900A operates exclusively in I/O mode on the phyCORE-ETH16, thus access occurs via eight 16-bit registers. Detailed information on this subject is contained in the CS8900A data sheet.

There are two LEDs on the PCB for the Link and LAN state display. The LEDs are positioned on the same side of the PCB as the RJ45 connector and can be connected for display within a housing encased area via an optical cable.

The phyCORE-ETH16 Adapter is mounted directly on the phyCORE LD (Low Density) module in question, whereby it immediately provides a fully configured Ethernet interface. The adapter is connected via the two 3-rowed, 2.54 mm pitch pin header connectors. No additional connections are required.

The following phyCORE-Modules are supported:

- phyCORE-PXAC37
- phyCORE-PXAG49

1.1 Block Diagram

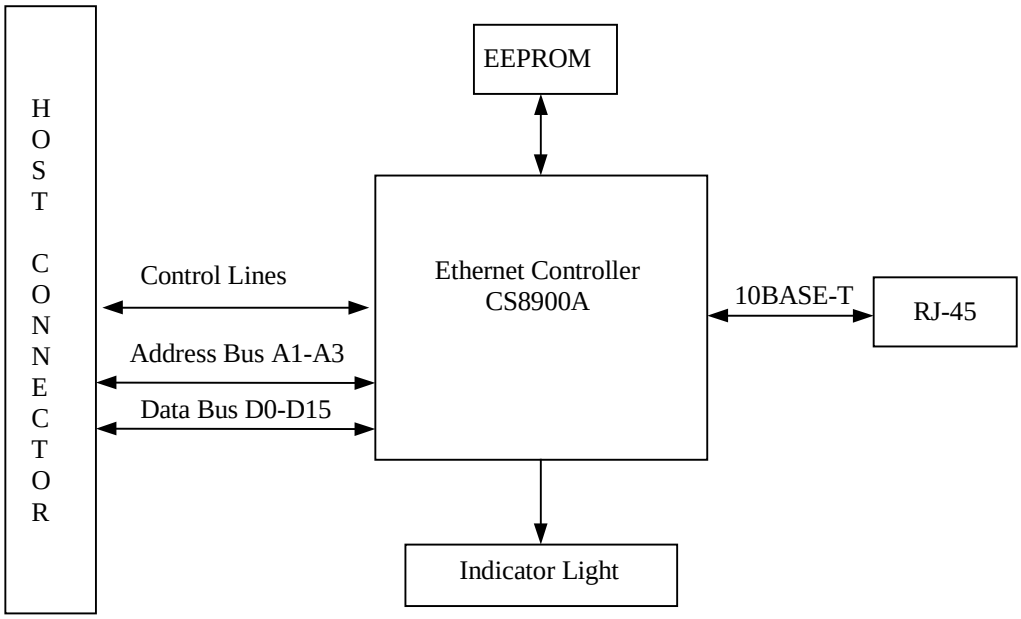

Figure 1: Block Diagram

1.2 View of the phyCORE-ETH16 Adapter

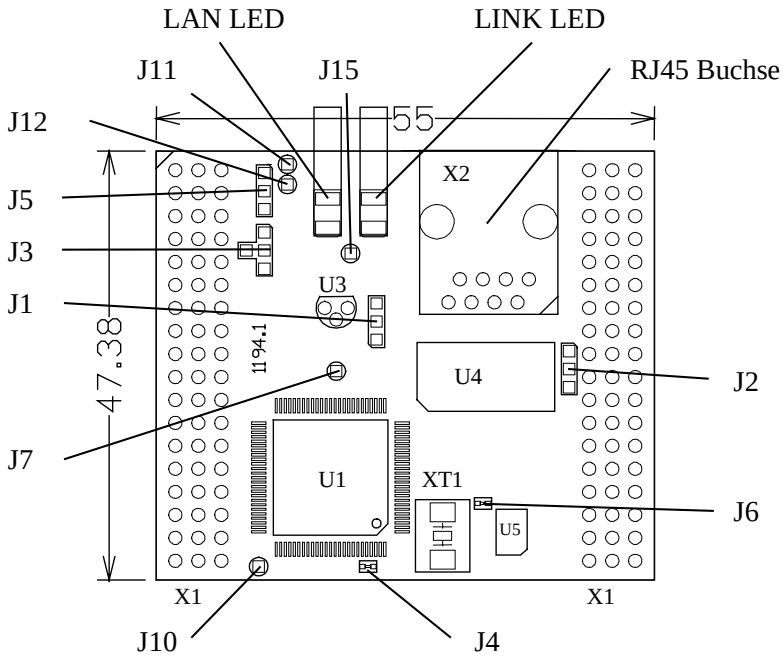

Figure 2: View of the phyCORE-ETH16 Adapter

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets located on the Spectrum CD. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to standard-width (2.54 mm / 0.1 in.) pin rows lining two sides the board (referred to as phyCORE-connector).

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the receptacle socket on the appropriate PHYTEC Development Board or your OEM application.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 3*).

The numbered matrix can be aligned with the phyCORE-ETH16 (viewed from above; phyCORE-connector header pins pointing down) or with the socket of the phyCORE Development Board LD 5V / target circuitry. The upper left-hand corner of the numbered matrix (Pin 1A) is thus covered with the corner of the phyCORE-ETH16 marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all contacts extend to the bottom of the board.

The numbering scheme is thus consistent for both the module's phyCORE-connector as well as mating connectors on the phyCORE Development Board LD 5V or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector's receptacle socket is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

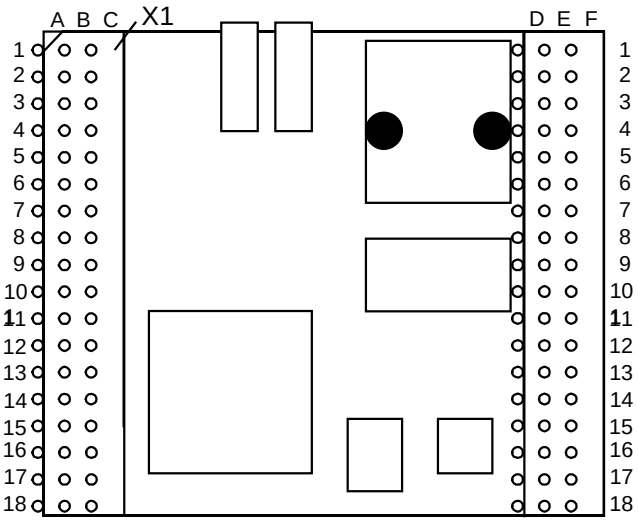

Figure 3: Numbered Matrix Overview of the phyCORE-Connector (Viewed from Above)

Table 1 provides an overview of the pinout of the phyCORE-connector

Pin Number	Signal	Pin Number	Signal
Pin Row X1A		**Pin Row X1D**	
1A	NC	1D	VCC
2A	IRQ1	2D, 3D, 4D, 5D, 6D	NC
3A	IRQ3	7D, 8D, 9D	GPIO1, GPIO2, GPIO4
4A	/CS2	10D, 11D, 12D, 13D, 14D, 15D	NC
5A	/RD	16D	D11
6A	NC	17D, 18D	NC
7A	A7		
8A, 9A, 10A, 11A, 12A	A5, A7, A10, A12, A15		
13A, 14A, 15A, 16A, 17A	D1, D3, D6, D8, D14		
18A	NC		
Pin Row X1B		**Pin Row X1E**	
1B	NC	1E	VCC
2B, 3B, 5B, 7B, 8B, 10B, 12B, 13B, 15B, 17B, 18B	GND	2E, 3E, 4E	NC
4B	NC	5E, 7E, 8E, 10E, 12E, 13E, 15E, 17E, 18E	GND
6B	A1	6E	/RESET
9B, 11B	NC	9E, 11E, 14E	NC
14B, 16B	D4, D9	16E	D12
Pin Row X1C		**Pin Row X1F**	
1C, 2C	IRQ0, IRQ2	1F, 2F, 3F	GND
3C, 4C	/CS1, /CS3	4F, 5F, 6F, 7F	NC
5C	/WRL	8F,	GPIO3
6C	A2	9F, 10F, 11F, 12F, 13F, 14F, 15F	NC
7C, 8C, 9C, 10C, 11C	NC	16F	D13
12C, 13C, 14C, 15C, 16C, 17C	D0, D2, D5, D7, D10, D15	17F, 18F	NC
18C	NC		

Table 1: Pinout of the phyCORE-Connector X1

3 Jumper

For configuration purposes, the phyCORE-ETH16 has 5 solder jumpers, some of which have been installed prior to delivery.

Figure 4: Numbering of the Jumper Pads

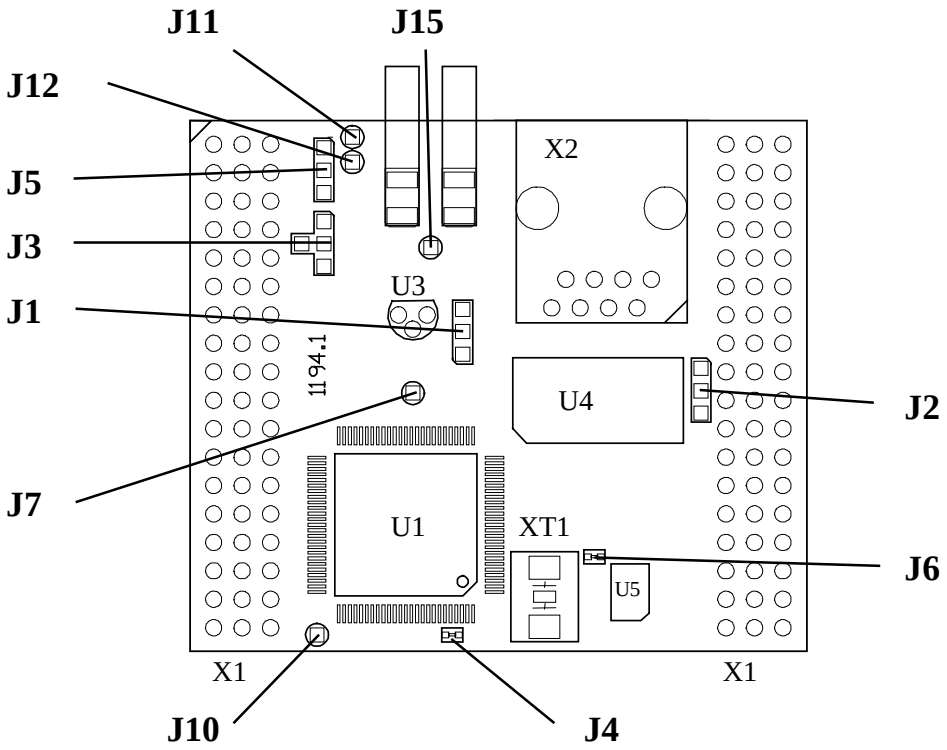

Figure 5: Location of the Jumpers (Top View)

The jumpers (J = solder jumper) have the following functions:

	Default Setting		**Alternative Setting**	
J1	(2 + 3)	GPIO3 connected with the DATA input of the DS2401 number chip	(1 + 2)	GPIO4 connected with the DATA input of the DS2401 number chip
J2	(1 + 2)	GPIO1 connected with the /SLEEP input of the CS8900A	(2 + 3)	GPIO2 connected with the /SLEEP input of the CS8900A
J3	(1 + 2)	/CS1 connected with the AEN and /SBHE input of the CS8900A	(2 + 3) (2 + 4)	/CS3 connected with the AEN and /SBHE input of the CS8900A /CS2 connected with the AEN and /SBHE input of the CS8900A
J4	(closed)	via printed PCB wire connects VCC and 5 V	(open)	seperation of printed PCB wire required alternative VCC Supply
J5	(1 + 2)	CS8900A Interrupt Request (INTRQ) connected with IRQ0 of the phyCORE	(2 + 3)	CS8900A Interrupt Request (INTRQ) connected with IRQ1 of the phyCORE

Table 2: Jumper Settings Overview

3.1 Data Line for Silicon Serial Number Chip J1

Communication to a DS2401 Silicon Serial Number can be implemented in various software applications for the definition of a node address or as copy protection in networked applications. The DS2401 in TO-92 packaging can be soldered on space U2. Solder Jumper J1 selects which of the GPIO (General Purpose Input Output) signals of the connected phyCORE module is used to access the DS2401 data input.

The following configurations are possible:

Data Input DS2401	J1
GPIO3 as DS2401 data input	2 + 3*
GPIO4 as DS2401 data input	1 + 2

*= Default Setting

Table 3: J1 Data Line of the Number Chip DS2401

3.2 Ethernet Controller Low-Power Mode J2

The CS8900A offers various low-power modes for power consumption critical applications. The phyCORE module's GPIO1 or GPIO2 (General Purpose Input Output) signals can be connected with the corresponding Ethernet controller input (/SLEEP) via Jumper J2.

The following configurations are possible:

Low Power Mode	J2
GPIO1 as /SLEEP input of the CS8900A	1 + 2*
GPIO2 as /SLEEP input of the CS8900A	2 + 3

*= Default Setting

Table 4: J2 /SLEEP Input of the Ethernet-Controllers

3.3 Ethernet Controller Addressing Mode J3

Using Jumper J3, it is possible to connect one of the phyCORE module's /CS signals simultaneously with the Address Enable bit (AEN) and the System Bus High Enable bit (/SBHE) of the CS8900A. We recommend putting the CS8900A into 16-bit mode by performing a dummy access to its memory space. As default, the Ethernet controller operates in 8-bit mode.

The following configurations are possible:

16-bit Mode Selection	J3
/CS1 connected to AEN and SBHE of the CS8900A	1 + 2*
/CS2 connected to AEN and SBHE of the CS8900A	2 + 4
/CS3 connected to AEN and SBHE of the CS8900A	2 + 3

*= Default Setting

Table 5: J3 Controlling the Signals AEN and SBHE

3.4 Solder Bridge for VCC Supply J4

The solder bridge J4 is used to establish a connection between the 5 V voltage and the VCC supply voltage of the Ethernet Adapter. This solder bridge is closed on the Ethernet Adapter at time of delivery.

3.5 Interrupt Request Selection J5

Jumper J5 connects the Interrupt Request (INTRQ) output on the CS8900A with the desired IRQ of the phyCORE module. Thus the Ethernet controller can generate an interrupt on the phyCORE module.

The following configurations are possible:

IRQ Signal Selection	J5
Interrupt Request (INTRQ) on CS8900A connected with phyCORE's IRQ0	1 + 2*
Interrupt Request (INTRQ) on CS8900A connected with phyCORE's IRQ1	2 + 3

*= Default Setting

Table 6: J5 Interrupt Request Selection

3.6 Solder Bridge for EEPROM Connection J6

The solder bridge J6 is used to establish a connection between the data ouptut of the EEPROM device on the module with the EEDI input of the CS8900A. This solder bridge is closed on the Ethernet Adapter at time of delivery.

Opening the solder bridge prevents reading of the EEPROM device contents. Thus the CS8900A will start with its default settings (address 300h, I/O mode).

There are various test points available on the phyCORE-ETH16 Ethernet Adapter for easy access to certain signals.

Test Point	Function
J7	Access of signal /IOCS16
J10	Access of signal /BSTATUS
J11	Access of signal IRQ2
J12	Access of signal IRQ3
J15	Access of signal LANLED

Table 7: Test Points on the phyCORE-ETH16

4 Display Units

Two LEDs are available on the phyCORE-ETH16 that are used for signaling various operating states.

LED	Description
D1	LANLED (CS8900A Pin LANLED – 100) Illuminates when sending and receiving data
D2	LINKLED (CS8900A Pin LINKLED - 99) Illuminates if there is an active connection via RJ45

Table 8: LEDs

The LEDs for LANLED and LINKLED are located next to the RJ45 connector and can be connected for display within a housing via an optical cable.

5 Technical Specifications

The phyCORE-ETH16 Adapter shown below in *Figure 6* in its physical dimensions. The module profile without pin header rows is approximately 15 mm. The component profile is approximately 2 mm on the underside of the PCB and 11.5 mm on the top side. The PCB itself is approximately 1.5 mm thick.

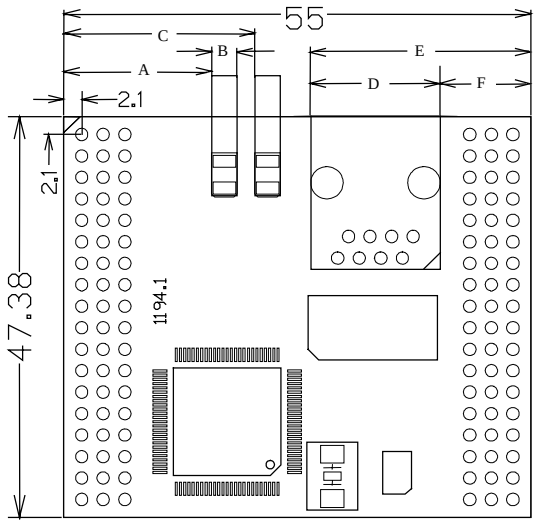

Figure 6: Physical Dimensions (not Shown at Scale)

All measurements in [mm]. Additional measurements are as follows:

A = 17 mm
B = 3 mm
C = 22 mm
D = 15 mm
E = 26 mm
F = 11 mm

Additional specifications:

- Dimensions: 55 mm x 47 mm ±0,01 mm
- Weight: approximately 23 g
- Storage temperature: -40°C to +90°C
- Operating temperature: 0°C to +70°C, extended -40°C to +85°C
- Humidity: maximum 95 % r.F. not condensed
- Operating voltage: 5 VDC ±10 %
- Power consumption: maximum 150 mA, typically 70 mA
- 10BASE-T interface: RJ45 jack for connection to an Ethernet hub via CAT 5 cable
- Mode display: 2 LEDs
  LINK-LED red
  LAN-LED green

These specifications describe the standard configuration of the phyCORE-ETH16 as of the printing of this manual.

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Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

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