Freescale Semiconductor
Addendum

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Errata to i.MX27 Multimedia Applications Processor Reference Manual, Rev. 0.3

This errata describes corrections to the *i.MX27 Multimedia Applications Processor Reference Manual*, Revision 0.3. For convenience, the section number and page number of the errata item in the reference manual are provided.

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17.5.3.2,17-19 In Table 17-13, “DSZ Bit Field Values,” update the 101 row, as follows. Note that only the updated row is shown:

Table 17-13. DSZ Bit Field Values

DSZ	Data Port Size	
	MUM=0	MUM=1
101	16-bit port, resides on DATA_IN/OUT [15:0] pins	Reserved

18.3.3.2,18-21 In Table 18-13, “ESDCFG0/ESDCFG1 Field Descriptions,” update t_{RC} row as follows. Note that only the updated row is shown:

Table18-13. ESDCFG0/ESDCFG1 Field Descriptions

Field	Description
3–0 t_{RC}	SDRAM Row Cycle Delay. This control field determines the minimum delay between a refresh and any subsequent refresh or read/write access. This delay corresponds to the minimum row cycle time captured in the t_{RC}/t_{RFC} memory timing specification. The value programmed in t_{RC} is the number of clocks inserted between the refresh and subsequent refresh/activate command. An example timing diagram for t_{RC} can be found in Figure 18-18. The bit field settings are listed on Table 18-16. **Note:** The t_{RC} control field is not used to enforce t_{RC} timing for row-activate to row-activate within the same bank as this is implicitly guaranteed by the sum of t_{RCD} + t_{CAS} + t_{RP}. Use regular paragraphs to summarize register function, then use the following special styles to define bit and field function. **Note:** Since t_{RC} + 1 is also used to determine the time between autorefresh cycles (may be referred to in memories as t_{RFC} or t_{ARFC}) and self-refresh exit time in SDR memories (may be referred to as t_{SREX} or t_{SRFX} for some vendors) and for a specific memory, these timings may be worse than t_{RC}, this parameter should be configured to the worst of the three, like so: t_{RFC} in controller = max(t_{ARFC}-1, t_{SRFX}-1, t_{RC} in memory). Example: For Samsung K4M51323PC-75 Mobile SDR SDRAM, t_{RC} is 72.5 ns, t_{ARFC} is 80 ns, and t_{SRFX} is 120 ns. At 133 MHz, cycle time is 7.5 ns, so t_{RC} = max(80/75.1 – 1, 120/7.5 – 1, 72.5/7.5) = 15 cycles.

18.3.3.2,18-30 Update Table 18-16, “t_{RC} Bit Field Encoding,” as follows:

Table 18-16. t_{RC} Bit Field Encoding

t_{RC}[3:0]	Delay
0000	20 clocks
0001	2 clocks
0010	3 clocks
0011	4 clocks
0100	5 clocks
0101	6 clocks
0110	7 clocks
0111	8 clocks
1000	9 clocks
1001	10 clocks
1010	11 clocks (reset value for CSD0)

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Table 18-16. t_{RC} Bit Field Encoding (continued)

t_{RC}[3:0]	Delay
1011	12 clocks
1100	13 clocks
1101	14 clocks
1110	15 clocks
1111	16 clocks

Chapter 25/25-1 In Figure 25-1, “KPP Peripheral Block Diagram,” update KDDR, KPCR, and KPDR from [5:8] to [15:8], as follows:

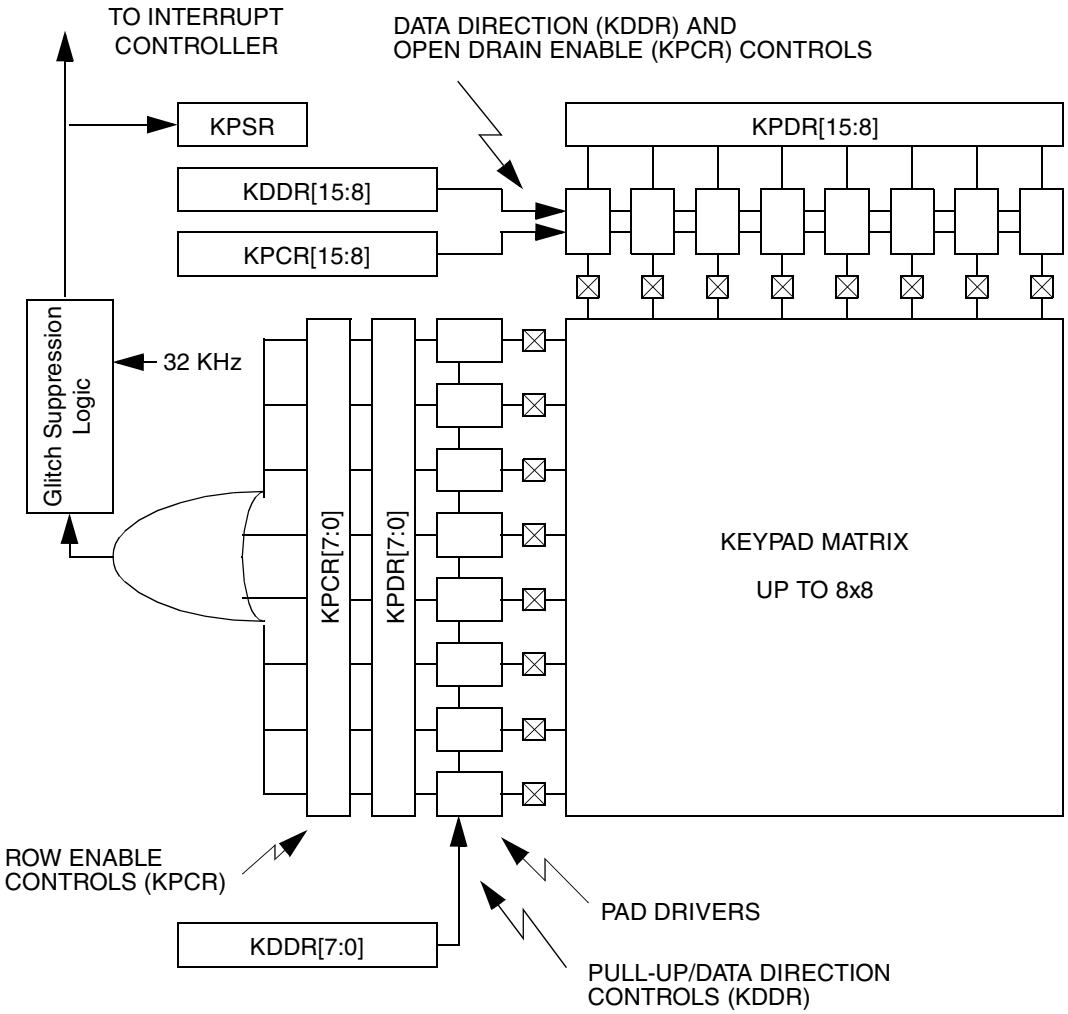

Figure 25-1. KPP Peripheral Block Diagram

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Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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