

ERRATA SHEET

Date: 2009 September 10

Document Release: Version 00.08

Device Affected: LPC3180/01

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2009 September 10

Document revision history

Rev	Date	Description
00.08	20090910	Second release
00.07	20080827	First Release

Identification:

The LPC3180/01 devices typically have the following top-side marking:

LPC3180FEL320/01

xxxxxxx

xxYYWWR

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC3180/01:

Revision Identifier (R)	Comment
'A'	Second device revision
' '	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
DDR.1	DDR interface has > 1.2 ns clock skew	'-', 'A'
RTC.1	An RTC match doesn't drive the ONSW pin active (high).	'-', 'A'
INT.1	GPI_08 does not generate in interrupt signal.	'-'

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
ESD.1	Weak ESD Protection on Reset_N Pin (pin AB16) protects up to 800V.	'-'

Errata Notes

Note	Short Description

Functional Problem Detail

DDR.1 DDR interface has >1.2ns clock skew

Introduction: DDR memory uses a differential clock which is generated by the LPC3180/01. The differential clock consists of two clock signals: EMC_CLK is the positive clock and DDR_nCLK is the negative clock.

Problem: There is approximately 1.27ns of skew between the low transition of the DDR_nCLK and the high transition of the EMC_CLK. This can cause two problems: 1) Some DDR devices use this clock transition to drive a digital lock loop (DLL) in the DDR device. The DDR clock skew can cause the DDR device's internal DLL to loose lock, resulting in the wrong data being latched. 2) The DDR clock skew can also cause a reduced Data Valid Window (also called Data-Out Window) from a DDR device. However, the LPC3180/01 has a programmable DQS delay to achieve center alignment for accurate data reads.

Work-around: Connecting the DDR device negative clock input (DDR_nCLK from the LPC3180/01) to the DDR Reference Voltage (Vref - the midpoint of the DDR signal voltage swing, which is generally VDDQ/2) avoids the clock skew problem, though it also eliminates the advantages of differential signaling. The LPC3180/01 DDR_nCLK output should be left unconnected. DDR Reference Voltage can be generated with a divide-by-two voltage divider. Standard DDR memories usually require a Vref input, so this DDR reference voltage should already be available. Mobile DDR devices typically do not have a Vref input, so the external voltage divider may need to be added to the design for this work-around.

It is also possible to compensate for the 1.27nS clock skew by adding an additional 7" of pcb trace length to the EMC_CLK signal. However, this could have unintentional consequences; such as increased Electro-Magnetic Interference.

RTC.1 An RTC match doesn't drive the ONSW pin active (high).

Introduction: An ONSW output pin (D12) is included in the LPC3180/01 to assist in waking up the chip after power is removed from all functions except the RTC and Battery RAM. When there is an active match condition the RTC will drive the ONSW pin high. The RTC only drives the ONSW pin while the match is active, and after 1 second of active match, if the software has not accessed the RTC block, the ONSW pin will go low when the match is no longer active.

Problem: When power is removed from all functions except the RTC and Battery RAM, the RTC does NOT drive the ONSW pin high when there is an active match condition.

Work-around: There is no work-around for this problem.

INT.1 GPI_08 does not generate an Interrupt signal.

Introduction: The LPC3180/01 contains 12 pins that can function as General Purpose Inputs(GPI_xx). Each of these pins can generate an individual interrupt for the input pin. The Sub Interrupt Controller 2 Enable register (SIC2_ER) contains bits that allow enabling or disabling the interrupt for the pin.

Problem: When bit nine is set to one in the The Sub Interrupt Controller 2 Enable register (SIC2_ER[9]) it does not enable the interrupt for the GPI_08 pin.

Work-around: There is no work-around for this problem.

AC/DC Deviation Detail

ESD.1 Weak ESD Protection on Reset_N Pad

Introduction: The LPC3180/01 was designed to withstand electrostatic discharges up to 2000 V using the Human Body Model.

Problem: The RESET_N pad (pin AB16) does not pass ESD tests above 800V.

Work-around: Observe proper ESD handling precautions for the RESET_N pin.