

AP16031

XC16x Family

Migration from C161/C164/C167
Microcontrollers to XC161/XC164/
XC167

Microcontrollers



Migration from C161/C164/C167 Microcontrollers to the XC161/XC164/XC167

Revision History: **2003-3**

V2.01

Previous Version: 1.1 -

Page	Subjects (major changes since last revision)
all pages	XC167 description added (January '03) and spelling checked
Page 36	3.10 RTC: Add advanced information 3.11 Parallel Port: Add Port 20, Port 0, Port 6 , Port 4 (XC164CS) pull up / pull down

This documentation is based on Data Sheets, Peripheral and System Specifications available in January 2003.

The latest documentation can be obtained on the internet.

<http://www.infineon.com/microcontrollers>

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



Table of Contents		Page
1	Introduction	5
1.1	Basic Features of XC161/164/167	5
1.2	Basic Features XC161 in Comparison with C161	7
1.3	Basic Features XC164 in Comparison with C164	10
1.4	Basic Features XC167 in Comparison with C167	13
1.5	Revision History	16
2	System Architecture	17
2.1	The Central Processing Units	17
2.2	Program and Data Memory Organization	18
2.3	External Bus Controller (EBC)	19
2.4	System Control Unit (SCU)	19
2.4.1	Reset Control Block	20
2.4.2	Central System Control Block	20
2.4.3	Power Management Control Block	23
2.4.4	Watchdog Timer	23
2.4.5	External Interrupt Control Block	24
2.5	Interrupt and PEC System	24
2.5.1	Interrupt controller	25
2.5.2	Peripheral Event Controller (PEC)	26
2.6	Traps	27
2.7	Revision History	28
3	On-Chip Peripheral Systems	29
3.1	Asynchronous/Synchronous Serial Interface (ASC)	29
3.2	High-Speed Synchronous Serial Interface (SSC)	30
3.3	Serial Data Link Module (SDLM)	30
3.4	Analog Digital Converter (ADC)	31
3.5	General Purpose Timer Units (GPT)	32
3.6	Capture/Compare Units	32
3.7	Enhanced Capture/Compare Unit 6	34
3.8	TwinCAN Module	34
3.9	IIC Bus	34
3.10	Real Time Clock (RTC)	35
3.11	Parallel Ports	36
3.12	Register Changes	37
3.13	Revision History	44
4	Migrating from C167CS/CR to XC167CI	45
4.1	Package Differences between C167 and XC167	45
4.2	Issues concerning alternate Port functions	48
4.3	Revision History	54
5	Additional Information	55

5.1	Power Supply	55
5.2	Power-up Sequence	56
5.3	Oscillator	57
5.4	Debug System	58
5.5	Revision History	58

6

1 Introduction

The XC161CJ, the XC164CS and the XC167CI are the first members of Infineon's new family of 16-bit microcontrollers based on the high-performance C166S V2 core in a sub-0.25 μ technology. For simplicity these various versions are referred to by the term XC161/164/167 within this Application Note, if not otherwise stated.

The C166S V2 core more than doubles the performance of the well established C166 core while still providing code compatibility. This document describes the modified functionalities and gives hints for porting an existing application from the C161/C164/C167 to the XC161/XC164/XC167.

1.1 Basic Features of XC161/164/167

High Performance 16-bit CPU

- 5-stage execution pipeline and a 2-stage instruction fetch pipeline with FIFO for instruction pre-fetching
- 25 ns single clock cycle instruction execution time at 40 MHz CPU clock
- nearly all instructions executed in one single CPU clock cycle
- one cycle multiplication (16 x16-bit)
- fast background execution of division (32-bit / 16-bit) in 21 CPU cycles
- Built-in advanced MAC unit
- accumulate instructions (MAC) executed in one CPU clock cycle
- Zero cycle jump execution
- 16 MByte total linear address space for code and data
- 2 additional fast register banks (NOT mapped in to RAM)
- Up to 64 Kbytes free locatable System Stack
- Stack address is extended to 24 bits
- Circular Stack mechanism is no more supported
- On Chip Emulation Support (OCE/OCDS) for full speed real time emulation

Integrated On-chip Memory

- 2-Kbyte dual-port RAM for variables, register banks, system stack (no code)
- 4-Kbyte (XC164: 2-Kbytes) additional high-speed data SRAM (no code)
- 2-Kbyte high-speed SRAM for code and data
- 128-Kbyte advanced Program Flash Memory for instruction code and constant data or 128-Kbyte ROM on XC164-16R

16 Priority-Level Interrupt System

- up to 128 interrupt sources with separate interrupt vectors on 16 priority levels and on 8 group levels
- Fast external interrupts (available for two interrupt sources with a priority higher than or equal to 12)
- Programmable location of vector table (in any 64K segment) and scaling

8-Channel Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)

- 24-bit source and destination pointers
- Enhanced PEC pointer Increment/Decrement Control
- Independently programmable PEC level and end of PEC interrupt

Intelligent On-chip Peripheral Subsystems

- 10-bit A/D Converter (XC161: 12-channel; XC164: 14-channel; XC167: 16-channel) with programmable conversion time (2 μ s minimum)
- Two Serial Interfaces (ASC0/1)
- 2 Multifunctional General Purpose Timer Units GPT1 and GPT2
- Two High Speed Synchronous Channel Interfaces (SSC0/1)
- Two 16-Channel Capture/Compare Units
- IIC Bus module with 10-bit addressing on XC161 and XC167
- TwinCAN module with two Full-CAN nodes
- Serial Data Link Module (SDLM), compliant with J1850 on XC161CJ-16F
- CAPCOM6E module with two independent timers dedicated to PWM generation for AC-motor control (XC164 and XC167)
- Real Time Clock (RTC)

Up to 103 IO Lines With Individual Bit Address ability

- Selectable input thresholds (not on all pins)
- Programmable driver characteristics
- I/O voltage is 5V (core/logic voltage is 2,5V)
- Push/pull or open drain output mode (not on P5)

Temperature Ranges

- 0 to +70°C, -40°C to +85°C, -40°C to +125°C

Table 1 Comparison of XC161 and C161 Continuation

XC161	C161
Zero cycle context switch with 2 new register banks (local register banks), not memory mapped using fast interrupt	Single cycle context switching support
16 bit extended stack pointer and a address extension to 24 bits by means of a 8-bit stack Segment register and Stack Overflow and Stack Underflow	System stack cache support with automatic stack overflow/underflow detection
Integrated On-chip Memory	Integrated On-chip Memory
2 Kbyte dual-port RAM for variables, register banks, system stack (no code)	2 Kbyte dual-port RAM (IRAM) for variables, register banks, system stack and code
4 Kbyte additional high-speed data SRAM (no code)	8 Kbyte on chip high-speed XRAM for code variables and user stack
2 Kbyte high-speed program SRAM for code and data	
128 Kbyte advanced Program Flash Memory for instruction code and constant data	256 Kbyte on chip Program Flash/ROM Memory for instruction code or constant data
16 Priority-Level Interrupt System	16 Priority-Level Interrupt System
74 interrupt nodes with separate interrupt vortors on 16 priority levels and on 8 group levels	up to 59 interrupt nodes with separate interrupt vortors on 16 priority levels and on 4 group levels
Fast external interrupts	Fast external interrupts
200 ns (8 cycle) typical interrupt latency in case of internal program and data execution	240/400 ns typical/maximum interrupt latency in case of internal program execution
8 channel Peripheral Event Controller (PEC)	8 channel Peripheral Event Controller (PEC)
Interrupt driven Single-Cycle Data Transfer	Interrupt driven Single-Cycle Data Transfer
Programmable PEC interrupt request level, from highest priority level 15 down to level 8	Programmable PEC interrupt request level, on highest priority level 15 and level 14
On-chip Peripheral Subsystems	On-chip Peripheral Subsystems
12-Channel 10-bit A/D Converter with programmable conversion time (2.55 μ s minimum @ 10-bit), auto scan mode, channel injection mode	12-Channel 10-bit A/D Converter with programmable conversion time (7.76 μ s minimum @ 10-bit), auto scan mode, channel injection mode

Table 1 Comparison of XC161 and C161 Continuation

XC161	C161
Two Serial Interfaces (ASC0/1)	Two Serial Interfaces (ASC0/1)
Two High Speed Synchronous Channel (SSC0/1)	High Speed Synchronous Channel (SSC0)
Two Multifunctional General Purpose Timer Units (GPT1 and GPT2)	Two Multifunctional General Purpose Timer Units (GPT1 and GPT2)
Two 16-Channel Capture/Compare Units	Two 16-Channel Capture/Compare Units
IIC Bus module with 10-bit addressing and 400Kbit/s	IIC Bus module with 10-bit addressing and 400Kbit/s
TwinCAN module with two full Full-CAN nodes	One or two on chip CAN Bus Modules Rev. 2.0B active
Serial Data Link Module (SDLM), compliant with J1850	Serial Data Link Module (SDLM), compliant with J1850
Real Time Clock (RTC)	Real Time Clock (RTC)
Up to 99 IO Lines With Individual Bit Addressability	Up to 93 IO Lines With Individual Bit Addressability
Selectable input thresholds (not on all pins)	Selectable input thresholds (not on pins)
Programmable driver characteristics	Programmable driver characteristics
Push/pull or open drain output mode (not on Port 5)	Push/pull or open drain output mode (not on Port 5)

Note: This comparison based on XC161 Target Spec, V1.1 Nov. 2000 and C161CS/JC/JI, V2.0 Jan 2001

1.3 Basic Features XC164 in Comparison with C164

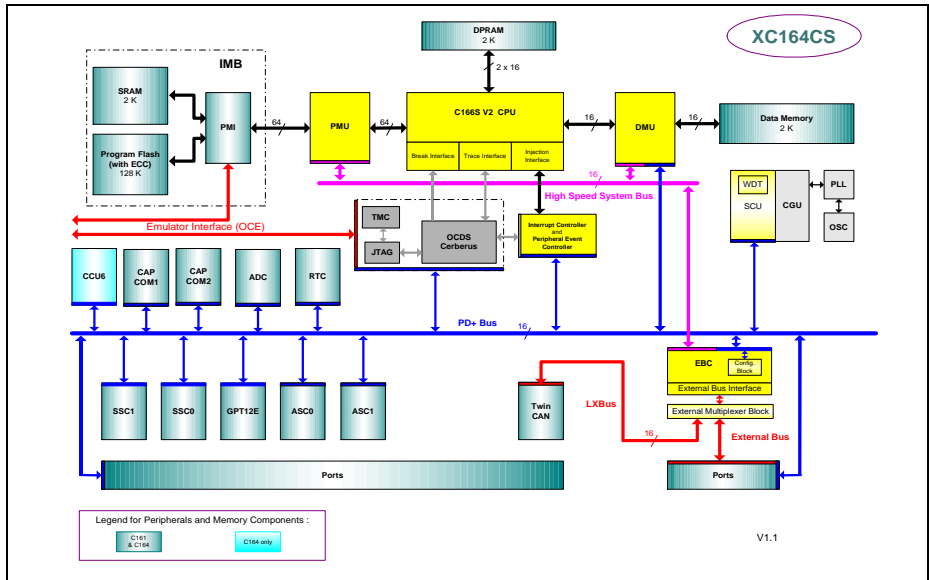


Figure 2 XC164CS Block Diagram

Table 1-1 Comparison of XC164 and C164

XC164		C164	
16-bit CPU		16-bit CPU	
5-stage execution pipeline and a 2-stage instruction fetch pipeline		4-stage Pipeline	
25 ns instruction execution time 40 MHz CPU clock	@	80 ns instruction execution time 25 MHz CPU clock	@
25 ns multiplication (16 x 16-bit) 40 MHz CPU clock	@	400 ns multiplication (16 x 16-bit) 25 MHz CPU clock	@
525 ns (21 CPU clock cycles) fast background division (32-bit / 16-bit)	@ 40 MHz CPU	800 ns division (32-bit / 16-bit) 25 MHz CPU clock	@
12 MByte total linear address space for code and data clock		16 MByte total linear address space for code and data	

Table 1-1 Comparison of XC164 and C164 Continuation

XC164	C164
Zero cycle context switch with 2 new register banks (local register banks), not memory mapped using fast interrupt	Single cycle context switching support
16 bit extended stack pointer and a address extension to 24 bits by means of a 8-bit Stack Segment register and Stack Overflow and Stack Underflow	System stack cache support with automatic stack overflow/underflow detection
Integrated On-chip Memory	Integrated On-chip Memory
2 Kbyte dual-port RAM for variables, register banks, system stack (no code)	2 Kbyte dual-port RAM (IRAM) for variables, register banks, system stack and code
2 Kbyte additional high-speed data SRAM (no code)	2 Kbyte high-speed XRAM for variables, user stack and code
2 Kbyte high-speed program SRAM for code and data	
128 Kbyte advanced Program Flash or ROM Memory for instruction code and constant data	64 Kbyte On-Chip Programm Flash or ROM memory
16 Priority-Level Interrupt System	16 Priority-Level Interrupt System
75 interrupt nodes with separate interrupt vertors on 16 priority levels and on 8 group levels	up to 33 interrupt nodes with separate interrupt vertors on 16 priority levels and on 4 group levels
Fast external interrupts	Fast external interrupts
200 ns (8 cycle) typical interrupt latency in case of internal program and data execution	240/400 ns typical/maximum interrupt latency in case of internal program execution
8 channel Peripheral Event Controller (PEC)	8 channel Peripheral Event Controller (PEC)
Interrupt driven Single-Cycle Data Transfer	Interrupt driven Single-Cycle Data Transfer
Programmable PEC interrupt request level, from highest priority level 15 down to level 8	Programmable PEC interrupt request level, from highest priority level 15 and level 14
On-chip Peripheral Subsystems	On-chip Peripheral Subsystems
14-Channel 10-bit A/D Converter with programmable conversion time (2.55 μ s minimum @ 10-bit), auto scan mode	8-Channel 10-bit A/D Converter with programmable conversion time (7,76 μ s minimum)
Two Serial Interfaces (ASC0/1)	One Serial Interfaces (ASC0)

Table 1-1 Comparison of XC164 and C164 Continuation

XC164	C164
Two High Speed Synchronous Channels (SSC0/1)	One High Speed Synchronous Channel (SSC0)
2 Multifunctional General Purpose Timer Units (GPT1 and GPT2)	2 Multifunctional General Purpose Timer Units (GPT1 and GPT2)
Two 16-Channel Capture/Compare Units	Two 16-Channel Capture/Compare Units
TwinCAN module (with 32 Message Objects, two full Full-CAN nodes)	On-chip CAN module (with 15 Message Objects, Full-CAN/Basic-CAN)
CAPCOM6E module with two independent timers dedicated to PWM generation for AC-motor control	CAPCOM6 module with two independent timers dedicated to PWM generation for AC-motor control
Real Time Clock (RTC)	Real Time Clock (RTC)
Up to 79 IO Lines With Individual Bit Addressability	Up to 59 IO Lines With Individual Bit Addressability
Selectable input thresholds (not on all pins)	Selectable input thresholds (not on all pins)
Programmable driver characteristics	Programmable driver characteristics
Push/pull or open drain output mode	Push/pull or open drain output mode

Note: This comparison is based on XC164CS Target Spec, V1.2 Jan. 2001 and C164 V2.0 Sep. 1999

1.4 Basic Features XC167 in Comparison with C167

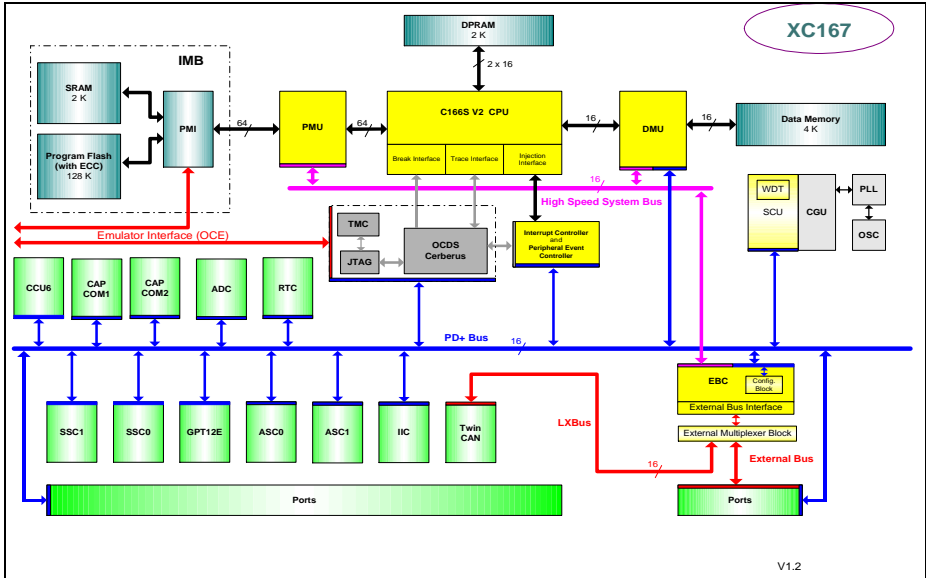


Figure 3 XC167CI Block Diagram

Table 2 Comparison of XC167 and C167

XC167		C167	
16-bit CPU		16-bit CPU	
5-stage execution pipeline and 2-stage instruction fetch pipeline		4-stage Pipeline	
25 ns instruction execution time @ 40 MHz CPU clock	@	80 minimum instruction execution time @ 25 MHz CPU clock (60 ns @ 33 MHz)	@
25 ns multiplication (16 x16-bit) @ 40 MHz clock	@	400 ns multiplication (16 x16-bit) @ 25 MHz CPU clock (300 ns @ 33MHz)	@
525 ns (21 CPU clock cycles) fast background division (32-bit / 16-bit) @ 40 MHz clock	@	800 ns division (32-bit / 16-bit) @ 25 MHz CPU clock (600 ns @ 33MHz)	@
12 MByte total linear address space for code and data		16 MByte total linear address space for code and data	

Introduction

XC167	C167
Zero cycle context switch with 2 new register banks (local register banks), not memory mapped using fast interrupt	Single cycle context switching support
16 bit extended stack pointer and a address extension to 24 bits by means of a 8-bit stack Segment register and Stack Overflow and Stack Underflow	System stack cache support with automatic stack overflow/underflow detection
Integrated On-chip Memory	Integrated On-chip Memory
2 Kbyte dual-port RAM for variables, register banks, system stack (no code)	3 Kbyte/ 2Kbyte dual-port RAM for code and data (C167CS/ C167CR)
4 Kbyte additional high-speed data SRAM (no code)	8 Kbyte/ 2Kbyte on chip high-speed XRAM for code variables and user stack (C167CS/ C167CR)
2 Kbyte high-speed program SRAM for code and data	
128 Kbyte advanced Program Flash Memory for instruction code and constant data	up to 32 Kbyte/ 128Kbyte on-chip ROM (C167CS/ C167CR)
16 Priority-Level Interrupt System	16 Priority-Level Interrupt System
73 interrupt nodes with separate interrupt vortors on 16 priority levels and on 8 group levels	up to 56 interrupt nodes with separate interrupt vortors on 16 priority levels and on 4 group levels
Fast external interrupts	Fast external interrupts
200 ns (8 cycle) typical interrupt latency in case of internal program and data execution	240 ns (180 ns)/ 400 ns (300 ns) typical/ maximum interrupt latency in case of internal program execution @ 25 MHz (33 MHz)
8 channel Peripheral Event Controller (PEC)	8 channel Peripheral Event Controller (PEC)
Interrupt driven Single-Cycle Data Transfer	Interrupt driven Single-Cycle Data Transfer
Programmable PEC interrupt request level, from highest priority level 15 down to level 8	Programmable PEC interrupt request level, on highest priority level 15 and level 14
On-chip Peripheral Subsystems	On-chip Peripheral Subsystems

Introduction

XC167	C167
16-Channel 10-bit A/D Converter with programmable conversion time (2.55 μ s minimum @ 10-bit), auto scan mode, channel injection mode	24-Channel 10-bit A/D Converter with programmable conversion time (7.76 μ s minimum @ 10-bit), auto scan mode, channel injection mode
Two Serial Interfaces (ASC0/1)	One Serial Interfaces (ASC0)
Two High Speed Synchronous Channel (SSC0/1)	One High Speed Synchronous Channel (SSC0)
Two Multifunctional General Purpose Timer Units (GPT1 and GPT2)	Two Multifunctional General Purpose Timer Units (GPT1 and GPT2)
Two 16-Channel Capture/Compare Units	Two 16-Channel Capture/Compare Units
IIC Bus module with 10-bit addressing and 400Kbit/s	
TwinCAN module with two full Full-CAN nodes	Two on chip CAN Bus Modules Rev. 2.0B active
CAPCOM6E module with two independent timers dedicated to PWM generation for AC-motor control	4-channel PWM unit
Real Time Clock (RTC) with dedicated oscillator and several interrupt possibilities	Real Time Clock (RTC)
Up to 103 IO Lines With Individual Bit Addressability	Up to 111 IO Lines With Individual Bit Addressability
Selectable input thresholds (not on all pins)	Selectable input thresholds (not on all pins)
Programmable driver characteristics	Programmable driver characteristics
Push/pull or open drain output mode (not on Port 5)	Push/pull or open drain output mode (not on Port 5)
Package Type	Package Type
144 pin TQFP Package	MQFP-144 Package

1.5 Revision History

Table 3 Changes V1.0 --> V2.0

Page	Description	Notes
Page 7	Added Figure 1 XC161CJ Block Diagram	14 Aug. 2001
Page 10	Added Figure 2 XC164CS Block Diagram	14 Aug. 2001
Page 13	Added Figure 3 XC167CI Block Diagram and XC167 Table	16 Jan 2003
(all tables above)	“Zero cycle context switch” entry modified	21 Jan 2003

2 System Architecture

The XC16x Controllers are improved and new-generation representatives of the Infineon full featured 16-bit single-chip CMOS microcontrollers. They combine the extended functionality and performance of the C166S V2 Core with powerful on-chip peripheral subsystems for example TwinCAN and memory units (e.g. embedded Flash).

Note: All Information in this Chapter are based on the Internal System Spec V1.1 Dec. 2000 and the user manuals V1.0

2.1 The Central Processing Units

C166SV2 is a member of the most recent generation of the popular C166 microcontroller cores. C166SV2 combines high performance with enhanced modular architecture. It was developed to provide easy migration from standard existing C16x controllers to the new C166SV2 core with its impressive DSP performance and advanced interrupt handling.

Instruction Set

- binary opcode compatible with C16x family
- not full source (or object) code compatible
- Additional instructions to support HLL and operating systems
- integrated DSP instruction set for internal MAC unit.

Note: New repeat mechanism for block loops (not compatible to C166, code rework required)

General Purpose Register Architecture

- Register-based design with multiple variable register banks

Note: Context switch needs 19 cycles.

- 2 additional register banks for fast context switching

Note: GPR_Bank1 and GPR_Bank2 are not mapped in Memory and can be used for fast context switching.

- 16 General-purpose registers (GPRs) for byte operands
- 16 General-purpose registers (GPRs) for integer operands
- Overlapping 8-bit and 16-bit registers
- Register-based design with multiple variable register banks (cached)

System Stack

- Up to 64 Kbytes free locatable System Stack (SPSEG register)
- Stack pointer is extended to 16 bit
- Stack address is extended to 24 bit (8-bit Stack Segment Register SPSEG)
- STKOV and STKUN became 16 bit wide and use SPSEG for address extension
- Stack Overflow and Stack Underflow are detected on all implicit accesses to the stack, i.e. PUSH, POP, CALL, RET (not by ALU Operations)
- no circular stack support

Note: Contrary to C166 behaviour, stack over- or underflows are not detected on explicit stack pointer manipulation (i.e. instructions ADD, SUB) .

2.2 Program and Data Memory Organization

The internal program memory is organized into the following memory blocks:

- 128 Kbyte program Flash memory (including error correction ECC)
- 2 Kbyte program SRAM
- 2 Kbyte dual Port RAM (no Code)
- 4 Kbyte (XC164: 2 Kbyte) additional high-speed data (no code) SRAM
- Startup ROM for Startup code (internal use)

Changes of address mapping

- Start address of internal program Flash/ ROM changed to segment 192 (C0'0000 H)
- Start address of internal boot sector changed to segment 191 (BF'0000 H)
- Additional start address of internal Program SRAM (E0'0000 H)
- No instruction execution out of data SRAM and of dual-port RAM
- 4K SFR space, called XSFR space, located in segment 0
- PEC source- and destination pointers now located in new XSFR space (new internal 4K I/O space, located in segment 0)
- All registers of External Bus Controller located in new XSFR space
- IIC, SDLM and CAPCOM6 registers located in new XSFR space

New features:

- New Register IMBCTR contains the bitfields controlling the wait state generation for the Flash memory and the other internal program memory blocks.

Note: Often used constants (like look-up tables) should be located (moved) into DPRAM to avoid code fetch delay caused by constant reading.

2.3 External Bus Controller (EBC)

The XC16x External Bus Controller (EBC) allows access to external peripherals/ memories and to internal LXBus modules. The LXBus is an internal representation of the External Bus and allows to access integrated peripherals and modules in the same way as external components. As some External Bus control signals are generally configurable, related additional control signals are necessary for the internal LXBus to support its maybe different configuration. The EBC is optimized for higher frequencies with a large granularity for low frequencies (bus signal control with one clock edge).

Note: *The XC16x derivatives provide a new enhanced register layout. The C16x registers SYSCON and BUSCONx are no longer used. But because the configuration of the external bus controller is done during the application initialization, only some initialization code has to be adapted for using the new EBC module instead of the C16x external bus controller. The basic and general behavior is now programmed via the mode-selection registers EBCMOD0 and EBCMOD1.*

New features:

- all external accesses outside of the CS-windows (XC161 and XC167: CS0..CS4 and XC164: CS0..CS3) are controlled via registers FCONCSx and TCONCSx

Note: *Ready pin and bus arbitration pins are not available on 100-pin package (XC164CS)*

Note: *For detailed information of register-bits, reset values and functions, please refer to the current system specification.*

2.4 System Control Unit (SCU)

The XC16x System Control Unit (SCU) summarizes a number of central control tasks and product specific features. The SCU sub-modules provide the following functions:

- Reset Control Block
- Central System Control Block
- Power Management Control Block
- Watchdog Timer
- External Interrupt Control Block

New features:

- Temperature Compensation Block

changed inadvertently. The unlock instruction sequence in the XC161/164/167 for registers with write protection (e.g. SYSCONn) has been improved.

The XC16x controllers provide three different security levels:

- Write Protected Mode (entered after the execution of EINIT): protected registers are locked against any write access (**read only**).
- Secured Mode (write access only with a special command sequence)
- Unprotected Mode (entered after reset)

Two mechanisms can be used to control the actual security level:

- Changing the security level
- Access in secured mode

For controlling the security level there are two separate **new** registers: The SCUSLC command register accepts the commands for manipulating the state machine and the read-only SCUSLS status register.

New features:

- all SCU registers are secured
- special command sequence includes a password
- The register protection mechanism is also available for registers outside of the SCU (A control output signal is provided for this purpose.)

Note: For detailed information of XC16x Security Mechanism, please refer to the current System Specification.

2.4.2.2 Clock generation control

The operating clock for the XC16x controllers is generated in several steps, so the clock generation path can be optimized to the respective operating conditions and requirements. The clock generation is controlled via the PLL control register PLLCON.

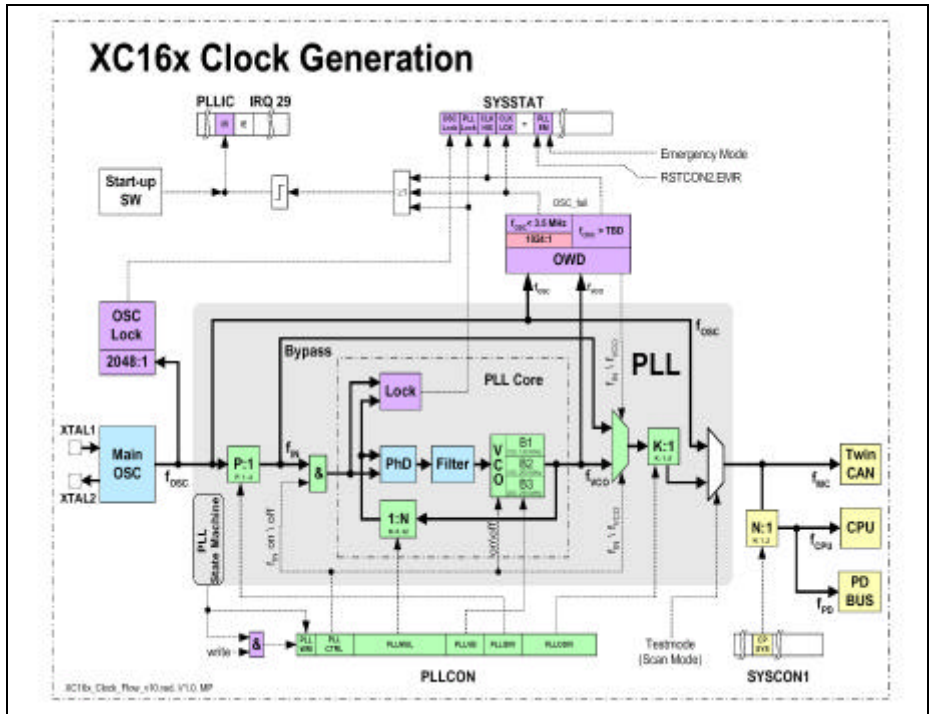


Figure 4 Clock generation control

Note: For clock configuration, please refer to the current system specification.

2.4.3 Power Management Control Block

The power consumption of the XC16x controllers can be reduced by several mechanisms. The level of power reduction depends on the level of system performance that is required under these circumstances. Some functions of the Power Management System have been simplified or improved.

New feature:

- new sleep mode has been introduced to offer improved capabilities (entered upon execution of the IDLE instruction)

Note: In Sleep mode clocking of all internal blocks (including WDT) is stopped. The contents of the internal RAM, however, are preserved through the voltage supplied via the V_{DD} pins.

Note: SYSCON2 register and Slow Down Divider is eliminated and a new PLL control register is included. The allocation of peripheral disable bits within register SYSCON3 is device specific and may be different in other derivatives than the XC161/164/167.

Note: For detailed information of register-bits and functions, please refer to the current System Specification.

2.4.4 Watchdog Timer

The Watchdog Timer of the XC16x controller works in compatible WDT mode in the same way like the C161 Watchdog. The software has to be designed to service the watchdog timer before it overflows.

Changes in WDTCON:

- The WDTIN-bit and WDTPRE-bit for Watchdog time ranges are combined to 2-bits in WDTIN
- Bits WDTR, SWR and HWR (SHWR and LHWR combined to HWR) move to the new SYSSTAT Register

New features:

- Enhanced mode: the Watchdog timer can be enabled and disabled at any time. For this ENWDT instruction is created and implemented as a protected instruction (the opcode 85h is no longer reserved)
- Enhanced mode is independent of the EINIT instruction

Note: XC16x Watchdog is clocked by the peripheral clock (C161 and C167: with CPU clock)

Note: A watchdog timer reset is unconditional. All current data/code accesses are aborted.

Note: For detailed information of register-bits and functions, please refer to the current System Specification.

2.4.5 External Interrupt Control Block

The major task of this block is the detection of external interrupt triggers. The source and the valid event for such a trigger are selectable. Besides this the SCU also combines the interrupt requests of some other modules before activating the respective interrupt nodes.

New Bits and **features** in known registers:

- register EXICON is complete with 4 new External Interrupt 4-7 Edge Selection Fields
- the structure of EXISEL register changed. An External Interrupt Source Field (0-7) is now 4 bits long. So EXISEL is divided in two registers, EXISEL0 and EXISEL1

Note: For detailed information of Register-bits, Reset Values and functions, please refer to the current System Specification.

2.5 Interrupt and PEC System

The Interrupt and Exception control system of the XC161/164/167 is responsible for managing all system and core exceptions. Four different kinds of exceptions are executed in a similar way:

- Interrupts generated by the Interrupt controller
- DMA transfers issued from the Peripheral Event Controller (PEC)
- Software Traps caused by the Trap instruction
- Hardware Traps issued by faults or specific system states

Changes:

- PEC source and destination pointer are located in the 4Kbytes I/O area
- extended group level and PEC interrupt subnode.
- Illegal External Bus Access TRAP is not supported
- Illegal Instruction Access Trap (branch to odd target address) is not supported.
- Interrupt/PEC-Controller is clocked with Peripheral clock, so a lower peripheral clock leads to increased interrupt prioritisation time!

2.5.1 Interrupt controller

The C166S V2 core provides up to 80 separate interrupt nodes that may be assigned to sixteen interrupt priority levels with 8 sub-priorities inside each level (group priority).

Changes in Interrupt controller:

The location of the vector table is programmable. The vector table can be located in all segments with exception of the reserved segment 191. For this feature the new VECSEG register is provided. It specifies the segment of the Vector Table. The VECSC bit field of the CPUCON1 register controls the number of word locations separating two vectors. The space between two vectors can be programmed to 2, 4, 8 or 16 words.

New feature:

For a very fast interrupt response time, XC16x controllers offer a new feature of the interrupt system-Interrupt Jump Table Cache (also called “fast interrupt”). The interrupt controller (ITC) can transfer a 24-bit vector to the CPU which is directly used as a start address for the service routine.

New Bits in known registers:

- register xxIC is extended with Bit 8 for Group Priority Extension

Note: The interrupt request line arbitration is clocked with Peripheral clock. Due to different pipeline and internal bus structure, the interrupt/ PEC response times are different from those of the C166 architecture. There are also some bit-changes in the Processor Status Word Register (PSW). However, the PSW is downwardly compatible.

Note: For detailed information of new registers and register-bits, reset values and functions , please refer to the current System Specification.

2.5.2 Peripheral Event Controller (PEC)

The Peripheral Event Controller (PEC) makes a decision about the CPU action required to manage an interrupt request. It may be either normal interrupt service or fast data transfer between two memory locations. The XC161/167 PEC controls 8 fast data transfer channels with 24-bit source and destination pointers.

New in PEC:

The PEC source and destination pointers consist of the 16-bit PEC source pointer register, a 16-bit PEC destination pointer register and a 16-bit segment pointer register. The segment pointer register consists of one 8-bit source and one 8-bit destination pointer Segment Addresses.

System Architecture

A new SBRK (software break) instruction has been introduced to ease the debug of an application (the opcode 8Ch is no longer reserved). It can be used to generate a hard-ware trap (Class A) by software. Its behaviour is closely linked to the On Chip Emulation module.

New Bits in known registers:

- Bits 0 and 1 in TFR are removed, bit 4 for Flash access error and Bit 12 for Software Break included

2.7 Revision History

Table 2-1 Changes V1.0 --> V1.1

Page	Description	Notes
Page 23	added sleep mode as new feature	10 Apr 2002
Page 23	feature WDT advanced	10 Apr 2002
Page 27	New software break instruction	11 Apr 2002
Page 19	change new feature, clear Note	25 Apr 2002
Page 22	Added Figure 4: Clock generation control	23 Jan 2003

Table 2-2 Changes V1.1 --> V2.0

Page	Description	Notes
Page 20	chapter advanced	4 Dec 2002
Page 26	added figure	4 Dez 2002

3 On-Chip Peripheral Systems

This chapter describes the on On-Chip Peripheral System of the XC161x controllers in comparison to the C166 Family. This On-Chip Peripherals are controlled either via the PD+Bus or the LXBus. The PD+Bus of XC16x is a derivative of the PD Bus from the C166, maintaining full functional compatibility. Each Peripheral has its own new Module Identification Register with a Module Identification Number and a Revision Number.

For more information on the PD+Bus and the LXBus, please refer to the XC161/164/167 Peripheral Specification.

Note: All Information in this Chapter based on the XC161/164 Peripherals Spec V1.1 Dec. 2000 and on the XC167 Manual V1.0

3.1 Asynchronous/Synchronous Serial Interface (ASC)

The Asynchronous/Synchronous Serial Interface provides serial communication between the XC16x and other microcontrollers, microprocessors or external peripherals. The implementation is similar to the implementation on C166 microcontrollers.

To work with the XC161/164/167 ASC in your project, please pay attention to the table "Register-Changes" at the end of this chapter.

Note: The module function will be controlled by the corresponding port pin via port alternate select register and port direction register.

New Bits in known registers:

- One new bit in XC161/164/167 ASC_x_CON. Bit 11 for Fractional Divider enable/disable. After reset the Fractional Divider is disabled.
- Interrupt control registers contain also a new Bit, Bit 8 for Group Priority Extension.

New features:

- Supports IrDA data transmission
- Autobaud Detection
- Transmission and reception of data can be FIFO-buffered.

Note: For detailed information of Register-bits, Reset Values and functions, please refer to the current Peripheral Specification of the respective controller.

3.2 High-Speed Synchronous Serial Interface (SSC)

The High-Speed Synchronous Serial Interface supports both full-duplex and half-duplex serial synchronous communication up to 20 Mbaud (40MHz module clock). FIFO buffering is not supported in this version.

To work with the SSC in your project, please pay attention to the table “Register-Changes” at the end of this chapter.

Note: *The module function will be controlled by the corresponding Port Pin via port alternate select registers and Port direction registers.*

New Bits in known registers:

- in XC161/164/167 SSC_CON (Enable-Bit = 0) there is a new Bit, Bit 7 for Loop Back Control. After Reset with normal output mode.
- Interrupt control registers contain a new Bit, Bit 8 for Group Priority Extension.

Note: *For detailed information of register-bits, reset values and functions, please refer to the current Peripheral Specification of the respective controller.*

3.3 Serial Data Link Module (SDLM)

The Serial Data Link Module (SDLM) provides serial communication to a J1850 based multiplexed bus via an external J1850 bus transceiver chip. The module is conforming to the SAE Class B J1850 specification and compatible to class 2 protocol.

To work with the XC161 SDLM in your project, please pay attention to the table “Register-Changes” at the end of this chapter.

Note: *The module function will be controlled by the corresponding port pin via port alternate select registers, SDLM_PISEL and port direction registers.*

New Bits in known registers:

- Bit 7 in GLOBCON is for passive bit select

Note: *For detailed information of register-bits, reset values and functions, please refer to the current XC161/164 Peripheral Specification.*

3.4 Analog Digital Converter (ADC)

For analog signal measurement, the XC16x controllers are equipped with a 8-bit/10-bit A/D Converter with up to 16 multiplexed input channels including sample and hold functionality. It uses the method of successive approximation. The conversion times of the ADC in the XC16x is shorter than in the C16x. However, similar conversion times can be achieved by configuring bit fields ADCTC and ADSTC in register ADC_CON.

To work with the ADC in your project, please pay attention to the table “Register-Changes” at the end of this chapter.

Table 4 Analog Digital Converter characteristics

Controller	Number of Channels	Port Pins
XC161	12 channels	AN0..7 (P5.0..7) AN12..15 (P5.12..15)
XC164	14 channels	AN0..7 (P5.0..7) AN10..15 (P5.10..15)
XC167	16 channels	AN0..15 (P5.0..15)

Note:

For XC161 package, 12 pins (P5.15-12 and P5.7-0) are available. For XC164 implementation (TQFP-100), 14 pins (P5.15-10 and P5.7-0) are available. So adjust the settings in the Digital Input Disable Register if required.

The C167CS supports up to 24 ADC channels. The XC167 provides 16 ADC channels. AN16..AN23 are not available.

ADCTC in ADC_CON is calculated with fper!

New Bits in known registers:

- Bit 12 and Bit 13 in XC161/164/167 ADCx_CON are for Sample Time Control. After reset the sample time takes 8 periods of ADC Basic Clock.
- Interrupt control register contains a new Bit, Bit 8 for Group Priority Extension.

New features:

- Automatic Self-Calibration to changing temperatures or process variations
- Auto-Power-Down Feature of the A/D Converter

Note: For detailed information of register-bits, reset values and functions, please refer to the current Peripheral Specification of the respective controller

3.5 General Purpose Timer Units (GPT)

The General Purpose Timer Unit (GPT12E) provides very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication and other purposes.

To work with the GPT unit in your project, please pay attention to the table “Register-Changes” at the end of this chapter.

Note: *The Module function will be controlled by the corresponding Port Pin via port alternate select registers and Port direction registers.*

New Bits in known registers:

- Bit 11 up to 15 in GPT12E_T3CON. With the function of bit 11 and 12 is a Timer Block Prescaler. After a reset timer 3 works maximum input frequency of $f_{per}/8$. Bit 13 is for timer edge detection, bit 14 for Timer 3 count direction change and bit 15 for Timer 3 rotation direction.
- Bits 9 and 12 up to 15 in GPT12E_T4CON and GPT12E_T4CON. Bit 9 is for timer remote control, after reset Timer/Counter is controlled by its own run bit. Bit 12 is for Timer Interrupt disable, bit 13 for timer edge detection, bit 14 for timer count direction change and bit 15 for timer rotation detection.
- Bit 5 in T5CON is additional to Timer 5 Mode control, bit 8 for Timer 5 external Up/down enable, bit 9 for Timer 5 Remote control, bit 11 for Timer 5 capture correction.
- Bit 8 in T6CON is for Timer 6 external up/down enable, bits 11 and 12 for timer block prescaler and bit 14 is Timer 6 clear bit.
- Interrupt control register contains a new Bit, Bit 8 for Group Priority Extension.

Note: *For detailed information of register-bits, reset values and functions, please refer to the current Peripheral Specification of the respective controller.*

3.6 Capture/Compare Units

The CAPCOM unit can capture the contents of a timer on specific internal or external events, or can compare a timer contents with given values and modify output signals in case of a match. With this mechanism it supports generation and control of timing sequences with a minimum of software intervention.

To work with the CAPCOM12 Unit in your project, please pay attention to the table “Register-Changes” at the end of this chapter.

Note:

- *The CAPCOM2 IO pins CC16IO-CC21IO are assigned to Port 8 in the existing C164. They are assigned to Port 9 in the XC161/164/167. The module function will be controlled by the corresponding port pin via port alternate select registers and port direction registers.*
- *Compared to C167, some of the CAPCOM2 IO pins are assigned to different ports on XC167. This might cause a conflict between required alternate port functions.*

Table 5 Possible conflicts due to different port assignment on XC167

CAPCOM2 Channel	Assignment C167CS/CR	Assignment C167CI	Possible Conflicts
CC0IO..CC7IO	P2.0..P2.8	P6.0..P6.7	<ul style="list-style-type: none"> • port 6 IO lines • chipselect functions • bus arbitration functions
CC8IO..CC15IO	P2.8..P2.15	P2.8..P2.15	
CC16IO..CC21IO	P8.0..P8.5	P9.0..P9.5	<ul style="list-style-type: none"> • IIC bus
CC22IO..CC23IO	P8.6..P8.7	P1L.7: CC22IO P1H.0: CC23IO	<ul style="list-style-type: none"> • port 1 IO lines • address lines • CAPCOM 6 unit • fast external interrupt 7
CC24IO..CC27IO	P1H.4..P1H.7	P1H.4..P1.H7	
CC28IO..CC21IO	P7.4..P7.7	P7.4..P7.7	<ul style="list-style-type: none"> • fast external interrupt 7

New Bits in known registers:

- Interrupt control registers contain a new Bit, Bit 8 for Group Priority Extension.

New features:

- The output register is doubled, for compatibility reasons the output latch is identical with the port latch and for platform reasons an additional output register is implemented in the CAPCOM in parallel to the port latch;
- Dedicated double register compare mode
- Single event mode
- I/O stagger disable function with enhanced resolution of CAPCOM

Note: For detailed information of register-bits, reset values and functions, please refer to the current XC161/164/167 Peripheral Specification.

3.7 Enhanced Capture/Compare Unit 6

The Enhanced Capture/Compare Unit 6 integrated in XC164 and XC167 provides two independent timers (T12, T13) which can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

To use this new Enhanced Capture/Compare Unit 6 please refer to the current Peripheral Specification of the respective controller.

Note:

- *In XC167, PWM module of C167 has been replaced by the Capture/Compare Unit 6 which provides extended functionality. Therefore a code redesign is needed!*
- *The output pins of CAPCOM 6 are assigned to Port 1 on XC167 whereas the output pins of the PWM module are assigned to Port 7 on C167.*

3.8 TwinCAN Module

The new TwinCAN module in the XC16x controllers is used instead of the standard CAN module. The TwinCAN module is comparable to the stand-alone CAN and to the CAN module which is used in the 32-bit family.

To use this new TwinCAN module please refer to the current Peripheral Specification of the respective controller.

3.9 IIC Bus

IIC supports a certain protocol to allow devices to communicate directly with each other via two wires. One line is responsible for clock transfer and synchronization (SCL), the other is responsible for the data transfer (SDA).

The IIC Bus module has been integrated in the XC167 controller, whereas the X167 does not include it.

To work with the XC161/167 IIC in your project, please pay attention to the table “Register-Changes” at the end of this chapter.

Note: The alternate input select function, controlled by the IIC module PISEL register, is not required for XC161CJ. Therefore, lines SDA_INBUSI[x] (x=0-2) are connected to SDA_INBUS0[x], and lines SCL_INBUSI[x] (x=0-2) are connected to SCL_INBUS0[x]. The module function will be controlled by the corresponded port pin via port alternate select registers, port direction registers and the port open drain control

register. The IIC Receive/Transmit Buffer (ICRTB from C161) were replaced by the RTBH and RTBL Register.

New Bits in known registers:

- Bits 3,6 and 7 in IIC_CFG is for pin selection
- Bits 13 and 14 in IIC_ADR is a predivider for baudrate generation and bit 15 for baudrate prescaler mode
- Bit 7 in IIC_ST is the Interrupt Request Bit for Data Transmission End, Bits 8-10 is a counter of transmitted bytes since last data interrupt, bit 15 is for Read Mirror Enable.
- Bits 8-15 in IIC_ST can also used as Write Mirror if Bit 15 in IIC_CON (WMEN) is set
- Bit 8 in IIC_CON is for ignore IRQE, bit 9 for Stop Master, bits 10 and 11 for length of the transmit buffer, bit 15 is for Write Mirror Enable.
- Bits 8-15 in IIC_CON can also used as Read Mirror if bit 15 in IIC_ST (RMEN) is set
- Interrupt control register contains a new bit, bit 8 for Group Priority Extension.

New features (compared to C164/161/167):

- Extended buffer allows up to 4 send/receive data bytes to be stored
- Dynamic access up to 3 physical IIC busses

Note: For detailed information of register-bits, reset values and functions, please refer to the current Peripheral Specification of the respective controller.

3.10 Real Time Clock (RTC)

The Real Time Clock (RTC) module is basically an independent timer chain and counts clock ticks. The base frequency of the RTC can be programmed via a reload counter. The RTC can work fully asynchronous to the system frequency and is optimized on low power consumption. The RTC still operates, if the rest of the system is already powered down (sleep mode).

To work with the RTC in your project, please pay attention to the table “Register-Changes” at the end of this chapter.

Note: RTC Control bits from SYSCON2 register on C166 family devices will be found in SYSCON0 and RTC_CON registers on the XC16x devices.

New Bits in known registers:

- Interrupt control register contains a new bit, bit 8 for Group Priority Extension.

New features:

- Alarm interrupt for wake up on a defined time
- Operates in synchronous and asynchronous mode
- Count input selectable through registers
- Due to its own power supply path, the RTC can operate independently from the system power.
- After power-on, the RTC module must be reset via bit RTCRST in register SYSCON0 by the initialization software, because by definition a device reset (hardware/software/watchdog reset) does not affect the RTC module

Note: For detailed information of register-bits, reset values and functions, please refer to the current Peripheral Specification of the respective controller.

3.11 Parallel Ports

All port lines have programmable alternate input or output functions associated with them. These alternate functions can be disabled/enabled manually. The disabled ports may be used as general purpose IO lines.

Some Port Changes

- Port 20 added to allow more General Purpose I/O in single chip mode
 - RD, WR, READY, ALE, EA, RSTOUT can be GP I/O
 - RD,WR,EA have internal pull-ups that are turned on during reset, and are switched off at the end of the internal reset phase
 - ALE has internal pull down that are turned on during reset, and are switched off at the end of the internal reset phase
- On XC164 P3.1, P3.2, P3.3, P3.4, P3.5, P3.7 cannot be used while in JTAG level 1 mode. P3.15 must be used (CLKOUT)
 - T6OUT, ASC1, CAPIN, T3OUT, T3UDE, T4IN, T2IN functions not available
- all potential chip select signals (P6.0..4, XC164: P4.0..3) have internal pull-ups that are turned on during reset, and are switched off at the end of the internal reset phase
- all PORT0 pins have internal pull-ups that are turned on during reset, and are switched off at the end of the internal reset phase (independent of the status of pin EA#)

JTAG is disabled by pulling pin 51 on XC161/167 or pin 36 on XC164 low

- JTAG enables emulation, allows debugging features like breakpoints and also provides access to SFR bits or internal memory.
- Resistor to ground should be provided on hardware to allow software development/ flash programming.
- Footprint for JTAG pins should be placed on target layout.

Note: Please pay attention when connecting JTAG Pins with external resistors. Specification IEEE1149 defines pullups/pulldowns for the interface signals. The XC167 has a

different pinout and package than the C167. These devices are NOT directly pin-compatible (see Chapter 4 for details).

3.12 Register Changes

Table 3-1 ASC Registers

Function	Register Names		Comment
	C16x	XC16x	
Serial Channel x Control Register	S1CON	ASCx_CON	rename register
Serial Channel x Baudrate Generator Reload Register	S1BG	ASCx_BG	rename register
Serial Channel x Receive Buffer Register	S1RBUF	ASCx_RBUF	rename register
Serial Channel x Transmit Buffer Register	S1TBUF	ASCx_TBUF	rename register
Serial Channel x Transmit Interrupt Control Register	XP4IC	ASCx_TIC	rename register
Serial Channel x Receive Interrupt Control Register	XP5IC	ASCx_RIC	rename register
Serial Channel x Error Interrupt Register	XP6IC	ASCx_EIC	rename register
Port alternate select register*	-	ALTSEL0P3	select your future function for ASC0/1
Port direction register*	DP3	DP3	select your port direction

* to setup your ASC module use the ASC0/ASC1 IO selection and setup table in your current XC161/164/167 Peripheral Specification.

Table 3-2 SSC Registers

Function	Register Names		Comment
	C16x	XC16x	
SSCx Control Register	SSCCON	SSCx_CON	- rename register
SSCx Baudrate Timer/Reload Register	SSCBR	SSCx_BR	- rename register
SSCx Transmit Buffer Register	SSCTB	SSCx_TB	- rename register
SSCx Receive Buffer Register	SSCRB	SSCx_RB	- rename register

Table 3-2 SSC Registers

Function	Register Names		Comment
	C16x	XC16x	
SSCx Transmit Interrupt Control Register	SSCTIC	SSCx_TIC	– rename register
SSCx Receive Interrupt Control Register	SSCRIC	SSCx_RIC	– rename register
SSCx Error Interrupt Control Register	SSCEIC	SSCx_EIC	– rename register
Port alternate select register*	-	ALTSEL0P3	– enable port pin control by SSC module.
Port alternate select register*	-	ALTSEL0P1H	– enable port pin control by SSC module.

* to setup your SSC module use the SSC0/SSC1 I/O selection and setup table in your current XC161/164/167 Peripheral Specification.

Table 3-3 ADC Register

Function	Register Names		Comment
	C16x	XC16x	
ADC Result Register	ADDAT	ADC_DAT	– rename register
ADC Result Channel Injection Register	ADDAT2	ADC_DAT2	– rename register
ADC Control Register	ADCON	ADC_CON	– rename register
ADC End of Conversion Interrupt Control Register	ADCIC	ADC_CIC	– rename register
ADC Converter Overrun Error Interrupt Control Register	ADEIC	ADC_EIC	– rename register

Table 3-4 CAPCOM12 Registers

Function	Register Names		Comment
	C16x	XC16x	
CAPCOM1 Mode Control Register 0... 3	CCM0... CCM3	CC1_M0... CC1_M3	- rename register
CAPCOM2 Mode Control Register 4... 7	CCM4... CCM7	CC2_M4... CC2_M7	- rename register
CAPCOM1 Register 0... 15	CC0... CC15	CC1_CC0... CC1_CC15	- rename register
CAPCOM2 Register 16... 31	CC16... CC31	CC2_CC16... CC2_CC31	- rename register
CAPCOM1 Interrupt Control Register 0... 15	CC0IC... CC15IC	CC1_CC0IC... CC1_CC15IC	- rename register
CAPCOM2 Interrupt Control Register 16... 31	CC16IC... CC32IC	CC2_CC16IC... CC2_CC32IC	- rename register
CAPCOM1 Timer 0 and Timer 1 Control Register	T01CON	CC1_T01CON	- rename register
CAPCOM1 Timer 0 Register	T0	CC1_T0	- rename register
CAPCOM1 Timer 0 Reload Register	T0REL	CC1_T0REL	- rename register
CAPCOM1 Timer 0 Interrupt	T0IC	CC1_T0IC	- rename register
CAPCOM1 Timer 1 Register	T1	CC1_T1	- rename register
CAPCOM1 Timer 1 Reload Register	T1REL	CC1_T1REL	- rename register
CAPCOM1 Timer 1 Interrupt	T1IC	CC1_T1IC	- rename register
CAPCOM2 Timer 7 and Timer 8 Control Register	T78CON	CC2_T78CON	- rename register
CAPCOM2 Timer 7 Register	T7	CC2_T7	- rename register
CAPCOM2 Timer 7 Reload Register	T7REL	CC2_T7REL	- rename register
CAPCOM2 Timer 7 Interrupt	T7IC	CC2_T7IC	- rename register
CAPCOM2 Timer 8 Register	T8	CC2_T8	- rename register
CAPCOM2 Timer 8 Reload Register	T8REL	CC2_T8REL	- rename register
CAPCOM2 Timer 8 Interrupt	T8IC	CC2_T8IC	- rename register

Table 3-5 GPT12E Registers

Function	Register Names		Comment
	C16x	XC16x	
GPT12E Timer 2 Register	T2	GPT12E_T2	– rename register
GPT12E Timer 3 Register	T3	GPT12E_T3	– rename register
GPT12E Timer 4 Register	T4	GPT12E_T4	– rename register
GPT12E Timer 5 Register	T5	GPT12E_T5	– rename register
GPT12E Timer 6 Register	T6	GPT12E_T6	– rename register
GPT12E Timer 2 Control Register¹	T2CON	GPT12E_T2CON	– rename register
GPT12E Timer 4 Control Register²	T4CON	GPT12E_T4CON	– rename register
^{1,2} T2/T4RC: Remote Control (bit 9)	no	selecte runbit by its own run bit or Timer 3	– new function bit
^{1,2} T2/T4IRDIS:Interrupt enable for Incremental Interface Mode (bit 12)	no	0: enable; 1:disable	– new function bit
GPT12E Timer 3 Control Register³	T3CON	GPT12E_T3CON	– rename register
^{1,2,3} BPS1: Prescaler 1: for T2, T3, T4 (bit 11-12) 00b:	factor=8	factor=8	
01b:		factor=4	– new Prescaler
10b:		factor=32	– new Prescaler
11b:		factor=16	– new Prescaler
^{1,2,3} T2/T3/T4EDGE: Edge Detection (bit 13)	no	0: no; 1: count edge was detected	– new function bit
^{1,2,3} T2/T3/T4CHDIR: Count Direction Change (bit 14)	no	0: no ; 1: a change in count direction was detected	– new function bit
^{1,2,3} T2/T3/T4RDIR:Rotation Direction (bit 15)	no	0: Count up; 1: Count down	– new function bit
GPT12E Timer 5 Control Register⁴	T5CON	GPT12E_T5CON	– rename register
⁴ T5RC: Remote Control (bit 9)	no	selecte runbit by its own run bit or Timer 6	– new function bit
⁴ T5CC: T5 Capture Correction (bit 11)	no	yes (T5 counte -1 bevor being captured)	– new function bit
⁴ T5SC: T5 Capture Mode (bit 15)	no	T5SC: T5 Capture Mode (bit 15)	– new function bit
GPT12E Timer 6 Control Register⁵	T6CON	GPT12E_T6CON	– rename register
^{4,5} BPS2: Prescaler 1: for T5, T6 (bit 11-12) 00b:	factor=4	factor=4	
01b:		factor=2	– new Prescaler
10b:		factor=16	– new Prescaler
11b:		factor=8	– new Prescaler
^{4,5} T5/T6CLR:T5 Clear (bit 14)	no	T5 is cleared on a capure event	– new function bit
GPT12E Timer 3 Interrupt Control Register	T3IC	GPT12E_T3IC	– rename register
GPT12E Timer 4 Interrupt Control Register	T4IC	GPT12E_T4IC	– rename register

Table 3-5 GPT12E Registers

Function	Register Names		Comment
	C16x	XC16x	
GPT12E Timer 2 Register	T2	GPT12E_T2	– rename register
GPT12E Timer 5 Interrupt Control Register	T5IC	GPT12E_T5IC	– rename register
GPT12E Timer 6 Interrupt Control Register	T6IC	GPT12E_T6IC	– rename register
GPT12E CAPREL Interrupt Control Register	CRIC	GPT12E_CRIC	– rename register
Port alternate select register*	-	ALTSEL0P3	– enable port pin control by GPT12 module
Port alternate select register*	-	ALTSEL1P3	– enable port pin control by GPT12 module

* to setup your GPT Module use the GPT1/GPT2 Selection and Setup Table in your current XC161/164/167 Peripheral Specification.

Table 3-6 SLDM Registers

Function	Register Names		Comment
	C161	XC161	
SDLM Global Control Register	GLOBCON	SDLM_GLOBCON	– rename register
SDLM Clock Divider Register	CLKDIV	SDLM_CLKDIV	– rename register
SDLM Transceiver Delay Register	TXDELAY	SDLM_TXDELAY	– rename register
SDLM In-Frame Response Value Register	IFR	SDLM_IFR	– rename register
SDLM Buffer Status Register	BUFFSTAT	SDLM_BUFFSTAT	– rename register
SDLM Transmission Status Register	TRANSSTAT	SDLM_TRANSSTAT	– rename register
SDLM Bus Status Register	BUSSTAT	SDLM_BUSSTAT	– rename register
SDLM Error Status Register	ERRSTAT	SDLM_ERRSTAT	– rename register
SDLM Buffer Control Register	BUFFCON	SDLM_BUFFCON	– rename register
SDLM Flag Reset Register	FLAGRST	SDLM_FLAGRST	– rename register

Table 3-6 SLDM Registers

Function	Register Names		Comment
	C161	XC161	
SDLM Interrupt Control Register	INTCON	SDLM_INTCON	– rename register
SDLM Transmit Data Register 0	TXD0	SDLM_TXD0	– rename register
SDLM Transmit Data Register 0	TXD2	SDLM_TXD2	– rename register
SDLM Transmit Data Register 0	TXD4	SDLM_TXD4	– rename register
SDLM Transmit Data Register 0	TXD6	SDLM_TXD6	– rename register
SDLM Transmit Data Register 0	TXD8	SDLM_TXD8	– rename register
SDLM Transmit Data Register 0	TXD10	SDLM_TXD10	– rename register
SDLM Bus Transmit Byte Counter	TXCNT	SDLM_TXCNT	– rename register
SDLM CPU Transmit Byte Counter	TXCPU	SDLM_TXCPU	– rename register
SDLM Receive Data Register 00	RXD00	SDLM_RXD00	– rename register
SDLM Receive Data Register 02	RXD02	SDLM_RXD02	– rename register
SDLM Receive Data Register 04	RXD04	SDLM_RXD04	– rename register
SDLM Receive Data Register 06	RXD06	SDLM_RXD06	– rename register
SDLM Receive Data Register 08	RXD08	SDLM_RXD08	– rename register
SDLM Receive Data Register 10	RXD10	SDLM_RXD10	– rename register
SDLM Receive Data Register 0	RXD10	SDLM_RXD10	– rename register
SDLM Receive Data Register 2	RXD12	SDLM_RXD12	– rename register
SDLM Receive Data Register 4	RXD14	SDLM_RXD14	– rename register
SDLM Receive Data Register 6	RXD16	SDLM_RXD16	– rename register
SDLM Receive Data Register 8	RXD18	SDLM_RXD18	– rename register
SDLM Receive Data Register 10	RXD110	SDLM_RXD110	– rename register
SDLM Bus Receive Byte Counter	RXCNT	SDLM_RXCNT	– rename register
SDLM CPU Receive Byte Counter	RXCPU	SDLM_RXCPU	– rename register
SDLM Bus Receive Byte Counter	RXCNTB	SDLM_RXCNTB	– rename register
SDLM Start-of-Frame Pointer Register	SOFPT	SDLM_SOFPT	– rename register
SDLM Interrupt Control Register	XP7IC	SDLM_IC	– rename register
Port Input Select Register*	-	SDLM_PISEL	– enable port pin control by SDLM module.
Port alternate select register*	-	ALTSEL0P4	– enable port pin control by SDLM module.
Port alternate select register*	-	ALTSEL1P4	– enable port pin control by SDLM module.
Port alternate select register*	-	ALTSEL0P7	– enable port pin control by SDLM module.

Table 3-6 SLDM Registers

Function	Register Names		Comment
	C161	XC161	
Port alternate select register*	-	ALTSEL0P9	- enable port pin control by SDLM module.
Port alternate select register*	-	ALTSEL1P9	- enable port pin control by SDLM module.

* to setup your SLDM module use the SLDM I/O selection and setup table in your current XC161 Peripheral Specification.

Table 3-7 IIC Bus Registers

Function	Register Names		Comment
	C161	XC161/167	
IIC Configuration Register	ICCFG	IIC_CFG	- rename register
IIC Control Register	ICCON	IIC_CON	- rename register
IIC Status Register	ICST	IIC_ST	- rename register
IIC Address Register	ICADR	IIC_ADR	- rename register
IIC Data Interrupt Control Register	XP0IC	IIC_DIC	- rename register
IIC Protocol Event Interrupt Control Register	XP1IC	IIC_PEIC	- rename register
Port alternate select register*	-	ALTSEL0P9	- enable port pin control by IIC module.
Port alternate select register*	-	ALTSEL1P9	- enables port pin control by IIC module.
Port direction register*	DP9	DP9	- select your port direction
Open Drain Control Register*	ODP9	ODP9	- enable port pin control by IIC module.

* to setup your IIC module use the IIC I/O Selection and setup table in your current XC161/XC167 Peripheral Specification.

Table 3-8 RTC Registers

Function	Register Names		Comment
	C16x	XC16x	
RTC Timer High Register	RTCH	RTC_RTCH	- rename register
RTC Timer Low Register	RTCL	RTC_RTCL	- rename register

Table 3-8 RTC Registers

Function	Register Names		Comment
	C16x	XC16x	
RTC Interrupt Subnote Register	ISNC	RTC_ISNC	- rename register
RTC Interrupt Control Register	XP3IC	RTC_IC	- rename register
T14 Register	T14	RTC_T14	- rename register
T14 Reload Register	T14REL	RTC_T14REL	- rename register

3.13 Revision History

Table 3-9 Changes V1.0 --> V2.01

Page	Description	Notes
Page 36	chapter advanced	4 Dec 2002
Page 36	3.10 RTC: Add advanced information 3.11 Parallel Port: Add Port 20, Port 0, Port 6 , Port 4 (XC164CS) pull up / pull down	Dec 2003

4 Migrating from C167CS/CR to XC167CI

The architecture of the XC167 is different from the C167 architecture. The XC167 offers a variety of new functions and enhancements of the standard peripherals. New features were included e.g. in the Asynchronous Serial Interface (ASCI), the Analog-to-Digital Converter (ADC) or the timers (GPT12E). New modules have been added (CAPCOM6 or IIC bus) whereas some modules of the C167CR/CS have been removed (e.g. the PWM unit).

Compared to the XC161 and XC164, the architectural modifications from C167 to the XC167 are stronger. For this reason a separate chapter is dedicated to the migration to the new device.

4.1 Package Differences between C167 and XC167

Compared to the C167, the XC167 is manufactured in a different package. The C167 is built into a MQFP144 package whereas for XC167 the smaller 144-pin TQFP package is used. The pinout is different, which means that the target board layout has to be modified.

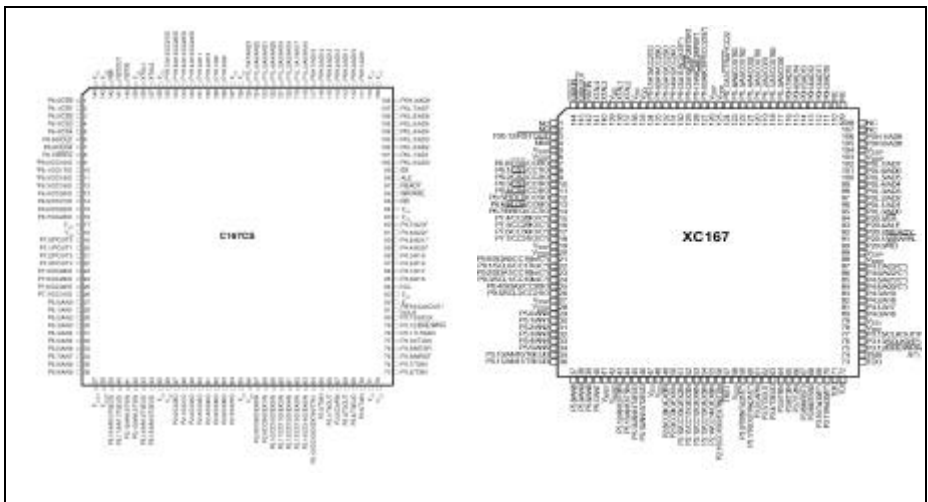


Figure 6 C167CS and XC167CI Package

Migrating from C167CS/CR to XC167CI
Table 6 Pin number modifications

Port Name / Pin Name	C167 (MQFP-144)	XC167 (TQFP-144)	Remarks
5V Supply Pins (VDD)	144, 136, 126, 109, 93, 82, 72, 56, 46, 17	(peripheral supply) 125, 103, 88, 58, 28, 20, 6	The XC167 needs dual voltage for core and peripherals. VDD and VSS are now split to VDDi, VSSi, VDDp and VSSp.
GND Pins (VSS)	143, 139, 127, 110, 94, 83, 71, 55, 45, 18	126, 104, 89, 27, 19, 6 (peripheral ground)	
Core voltage supply		48, 78, 135	the XC167 needs 2,5V core voltage
Core GND (VSSi)		47, 79, 136, 139	
XTAL 1	138	138	
XTAL 2	137	137	
XTAL 3		140	Input to the auxiliary (32-kHz) oscillator amplifier (RTC)
XTAL 4		141	Output of the auxiliary (32-kHz) oscillator amplifier (RTC)
VAREF	37	41	
VAGND	38	42	
Port 0	100-108, 111-117, 105-106	95-102, 111-116	
Port 1	118-125, 128-135	117-124, 127-134	ADC Channels AN16..AN23 (C167CS) are not available on XC167.
Port 2	47-54, 57-64	49-56	On XC167, Port 2 is an 8-bit port. (16-bit port on C167)
Port 3	65-70, 73-80, 81	59-70, 75-77,	
Port 4	85-92	80-87	
Port 5	27-36, 39-44	29-36, 37-40, 43-46	

Migrating from C167CS/CR to XC167CI
Table 6 Pin number modifications

Port Name / Pin Name	C167 (MQFP-144)	XC167 (TQFP-144)	Remarks
Port 6	1-8	Pin 7-15	Port 6 is shared with CAPCOM12 Unit. If chip select signals are used, e.g. CC0IO - CC4IO are not available.
Port 7	19-26	15-18	On XC167 Port 7 is a 4-bit port (8-bit on C167). P7.0-P7.3 are not available. POUT0-POUT3 (PWM output) are not available. Use e.g. CAPCOM6 features as a replacement.
Port 8	9-16	21-26	8-Bit Port Port 8 has been replaced by 6-Bit port Port 9.
TCK, TDI, TDO, TMS, BRKIN, BRKOUT		71, 72, 73, 74, 143, 144	On-Chip-Debugging System pins. (See IEEE1149 specification for pullup/pulldown resistors)
$\overline{\text{TRST}}$		57	Test-System Reset Input. A high level at this pin activates the XC167's debug system.
NMI	142	4	
$\overline{\text{RSTIN}}$	140	142	
$\overline{\text{RSTOUT}}$	141	3	$\overline{\text{RSTOUT}}$ (P20.12) can be used as general purpose IO pin on XC16x controllers.
NC	84	1, 2, 107, 108, 109, 110	do NOT connect these pins.
$\overline{\text{RD}}$, $\overline{\text{WR}}$ / $\overline{\text{WRL}}$, $\overline{\text{READY}}$, $\overline{\text{ALE}}$, $\overline{\text{EA}}$	95, 96, 97, 98, 99	90, 91, 32, 93, 94	Bus control pins (P20.0 - P20.5) can be used as general purpose IO pins on XC16x controllers.

4.2 Issues concerning alternate Port functions

The majority of the XC167 pins offer different functions. Normally a choice between different alternate functions is possible. However, only ONE alternate function can be selected at a time.

Migrating from C167CS/CR to XC167CI

Compared to C167, some alternate functions of the XC167 are assigned to different ports. Consequently in a small number of cases two functions used by the application might be the alternate function of ONE port pin. In this case a decision has to be made which function will be used and which one can be assigned to a different port pin. If this happens change of hard- and software is needed. The following table describes the chances of alternate port functions in detail.

Table 7 Port Functions Assignment

Port name	C167CS	C167CR	XC167CI
Port 0	POL.0-POL.7: IO POH.0-POH.7: IO Alternate Function 1 Address/ Data Bus lines. (See specification)	POL.0-POL.7: IO POH.0-POH.7: IO Alternate Function 1 Address/ Data Bus lines. (See specification)	POL.0-POL.7: IO POH.0-POH.7: IO Alternate Function 1 Address/ Data Bus lines. (See specification)

Migrating from C167CS/CR to XC167CI
Table 7 Port Functions Assignment

Port name	C167CS	C167CR	XC167CI
Port 1	P1L.0-P1L.7: IO P1H.0-P1H.7: IO Alternate Function 1 Address Bus Alternate Function 2 P1L.0-P1L.7: AN16-AN23 P1H.4-P1H.7: CC24IO-CC27IO	P1L.0-P1L.7: IO P1H.0-P1H.7: IO Alternate Function 1 Address Bus Alternate Function 2 P1H.4-P1H.7: CC24IO-CC27IO (capture input only)	P1L.0-P1L.7: IO P1H.0-P1H.7: IO Alternate Function 1 Address Bus Alternate Function 2 P1L.0: CC60 P1L.1: COUT60 P1L.2: CC61 P1L.3: COUT61 P1L.4: CC62 P1L.5: COUT62 P1L.6: COUT63 P1L.7: CTRAP <u>P1H.0: CC6POS0</u> <u>P1H.1: CC6POS1</u> P1H.2: CC6POS2 P1H.4-P1H.7: CC24IO-CC27IO Alternate Function 3 P1L.7: CC22IO P1H.0: CC23IO P1H.1: MRST1 P1H.2: MTSR1 P1H.3: SCLK1 Alternate Function 4 P1H.0: EX0IN (alternate Pin B) P1H.3: EX0IN (alternate Pin A)
Port 2	P2.0-P2.15: IO Alternate Function 1 P2.0-P.15: CC0IO-CC15IO Alternate Function 2 P2.8-P.15: EX0IN-EX7IN	P2.0-P2.15: IO Alternate Function 1 P2.0-P.15: CC0IO-CC15IO Alternate Function 2 P2.8-P.15: EX0IN-EX7IN	P2.8-P2.15: IO Alternate Function 1 P2.8-P.15: CC8IO-CC15IO <i>Note: CC0IO..CC7IO are assigned to port 6.</i> Alternate Function 2 P2.8-P.15: EX0IN-EX7IN <i>Note: Port 2 on XC167CI is an 8-bit port(16 bit on C167CR/CS).</i>

Migrating from C167CS/CR to XC167CI
Table 7 Port Functions Assignment

Port name	C167CS	C167CR	XC167CI
Port 3	P3.0-P3.14, P3.15: IO Alternate Function 1 P3.0: T0IN P3.1: T6OUT P3.2: CAPIN P3.3: T3OUT P3.4: T3EUD P3.5: T4IN P3.6: T3IN P3.7: T2IN P3.8: MRST P3.9: MTSR P3.10 TxD0 P3.11 <u>RxD0</u> P3.12 <u>BHE</u> or <u>WRH</u> P3.13 SCLK P3.15 CLKOUT/ FOUT	P3.0-P3.14, P3.15: IO Alternate Function 1 P3.0: T0IN P3.1: T6OUT P3.2: CAPIN P3.3: T3OUT P3.4: T3EUD P3.5: T4IN P3.6: T3IN P3.7: T2IN P3.8: MRST P3.9: MTSR P3.10 TxD0 P3.11 <u>RxD0</u> P3.12 <u>BHE</u> or <u>WRH</u> P3.13 SCLK P3.15 CLKOUT	P3.0-P3.14, P3.15: IO Alternate Function 1 P3.0: T0IN P3.1: T6OUT P3.2: CAPIN P3.3: T3OUT P3.4: T3EUD P3.5: T4IN P3.6: T3IN P3.7: T2IN P3.8: MRST0 P3.9: MTSR0 P3.10 TxD0 P3.11 <u>RxD0</u> P3.12 <u>BHE</u> or <u>WRH</u> P3.13 SCLK0 P3.15 CLKOUT/ FOUT Alternate Function 2 P3.0: TxD1 P3.1: RxD1 P3.10 EX2IN (alternate pin B) P3.11 EX2IN (alternate pin A) P3.12 EX3IN (alternate pin B) P3.13 EX3IN (alternate pin A) P3.15 CLKOUT/ FOUT

Migrating from C167CS/CR to XC167CI
Table 7 Port Functions Assignment

Port name	C167CS	C167CR	XC167CI
Port 4	P4.0-P4.7: IO Alternate Function 1 P4.0-P4.7: A16-A23 Alternate Function 2 P4.4: CAN2_RxD P4.5: CAN1_RxD P4.6: CAN1_TxD or CAN2_TxD P4.7: CAN1_RxD or CAN2_TxD or CAN2_RXD	P4.0-P4.7: IO Alternate Function 1 P4.0-P4.7: A16-A23 Alternate Function 2 P4.5: CAN1_RxD P4.6: CAN1_TxD	P4.0-P4.7: IO Alternate Function 1 P4.0-P4.7: A16-A23 Alternate Function 2 P4.4: CAN2_RxD P4.5: CAN1_RxD P4.6: CAN1_TxD P4.7: CAN1_TxD or CAN2_TxD Alternate Function 3 P4.4: EX5IN (alternate pin B) P4.5: EX4IN (alternate pin B) P4.6: EX5IN (alternate pin A) P4.7: EX4IN (alternate pin A)
Port 5	P5.0-P5.15: Input Alternate Function 1 P5.0-P5.15: AN0-AN15 Alternate Function 2 P5.10 T6EUD P5.11 T5EUD P5.12 T6IN P5.13 T5IN P5.14 T4EUD P5.15 T2EUD	P5.0-P5.15: Input Alternate Function 1 P5.0-P5.15: AN0-AN15 Alternate Function 2 P5.10 T6EUD P5.11 T5EUD P5.12 T6IN P5.13 T5IN P5.14 T4EUD P5.15 T2EUD	P5.0-P5.15: Input Alternate Function 1 P5.0-P5.15: AN0-AN15 Alternate Function 2 P5.10 T6EUD P5.11 T5EUD P5.12 T6IN P5.13 T5IN P5.14 T4EUD P5.15 T2EUD

Migrating from C167CS/CR to XC167CI
Table 7 Port Functions Assignment

Port name	C167CS	C167CR	XC167CI
Port 6	P6.0-P6.7: IO Alternate Function 1 P6.0-P6.4: <u>CS0, CS1,</u> <u>CS2, CS3, CS4</u> P6.5-P6.7: <u>HOLD,</u> <u>HLDA, BREQ</u>	P6.0 - P6.7: IO Alternate Function 1 P6.0 - P6.4: <u>CS0, CS1,</u> <u>CS2, CS3, CS4</u> P6.5 - P6.7: <u>HOLD,</u> <u>HLDA, BREQ</u>	P6.0 - P6.7: IO Alternate Function 1 P6.0 - P6.4: <u>CS0, CS1, CS2,</u> <u>CS3, CS4</u> P6.5-P6.7: <u>HLD, HOLDA,</u> <u>BREQ</u> Alternate Function 2 P6.0 - P6.7: CC0IO, CC1IO, CC2IO, CC3IO, CC4IO, CC5IO, CC6IO, CC7IO
Port 7	P7.0-P7.7: IO Alternate Function 1 P7.0-P7.3: POUT0, POUT1, POUT2, POUT3 P7.4-P7.7: CC28IO, CC29IO, CC30IO, CC31IO	P7.0-P7.7: IO Alternate Function 1 P7.0-P7.3: POUT0, POUT1, POUT2, POUT3 P7.4-P7.7: CC28IO, CC29IO, CC30IO, CC31IO	P7.4-P7.7: IO Alternate Function 1 P7.4-P7.7: CC28IO, CC29IO, CC30IO, CC31IO Alternate Function 2 P7.4: CAN2_RxD P7.5: CAN2_TxD P7.6: CAN1_RxD P7.7: CAN1_TxD Alternate Function 3 P7.4-P7.5: EX7IN, EX6IN (alternate pin B) P7.6-P7.7: EX7IN, EX6IN (alternate pin A) <i>Note: Port 7 on XC167CI is a 4-bit port (8-bit on C167CR/CS).</i>

Migrating from C167CS/CR to XC167CI

Table 7 Port Functions Assignment

Port name	C167CS	C167CR	XC167CI
Port 8 (Port 9)	P8.0-P8.7: IO Alternate Function 1 P8.0-P8.7: CC16IO, CC17IO, CC18IO, CC19IO, CC20IO, CC21IO, CC22IO, CC23IO Alternate Function 2 P8.0: CAN1/2_RxD P8.1: CAN1/2_TxD P8.2: CAN1/2_RxD P8.3: CAN1/2_TxD	P8.0-P8.7: IO Alternate Function 1 P8.0-P8.7: CC16IO, CC17IO, CC18IO, CC19IO, CC20IO, CC21IO, CC22IO, CC23IO	P9.0-P9.5: IO Alternate Function 1 P9.0-P9.5: CC16IO, CC17IO, CC18IO, CC19IO, CC20IO, CC21IO Alternate Function 2 P9.0 CAN2_RxD P9.1 CAN2_TxD P9.2 CAN1_RxD P9.3 CAN1_TxD Alternate Function 3 P9.0 SDA0 P9.1 SCL0 P9.2 SDA1 P9.3 SCL1 P9.4 SDA2 P9.5 SCL2 <i>Note: Port 9 of XC167CI (6-bit) has similar functions as Port 8 of XC167CR/CS (8-bit).</i>

This Chapter is based on the information provided in XC167 Data Sheet V1.0, C167CS-4R/L Data Sheet V2.2 and C167CR/SR Data Sheet V3.2

4.3 Revision History

Table 4-1 Changes V1.0 --> V2.0

Page	Description	Notes
Page 45	chapter added	6 Feb 2003

5 Additional Information

5.1 Power Supply

General Power Supply

The XC161/164/167 power supply concept uses different voltages for the core and for the pads.

Dual voltage power supply required:

- 5V for I/O, ADC, and port structures (Vddp)
- 2.5V for internal core, and XTAL (Vddi)

A power regulator is available from Infineon Technologies.

The TLE 7469 is a monolithic integrated voltage regulator with two voltage outputs specially designed to supply microcontrollers with dual supply voltage like the Infineon XC16x family. The voltage regulator features an integrated reset circuitry which monitors the supply voltage. At power-on the device checks both supply voltages and performs the power-on reset with an adjustable delay time. The voltage difference is kept in the range even during power-on and power-down time enabling save μC operation without external clamping. Using the integrated early warning comparator an external voltage can be supervised. An integrated output sink current circuitry keeps the controller's peripheral voltage below 5.5V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage. The regulator can be shut down via the Inhibit input. The TLE 7469 is designed for use under the severe conditions of automotive applications, and is therefore equipped with protection functions against over load, short circuit and over temperature.

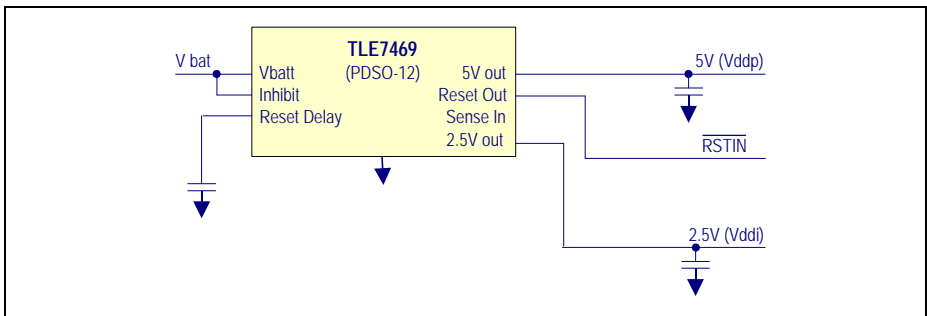


Figure 8 Dual Low-Drop Voltage Regulator TLE7469

5.2 Power-up Sequence

During power-up the reset pins $\overline{\text{RSTIN}}$ and $\overline{\text{TRST}}$ have to be held active until both power supply voltages have reached at least their minimum values. During the power-up time (rising of the supply voltages from 0 to their regular operating values) it has to be ensured, that V_{DDP} is never lower than $V_{\text{DDI}} - 0,5\text{V}$.

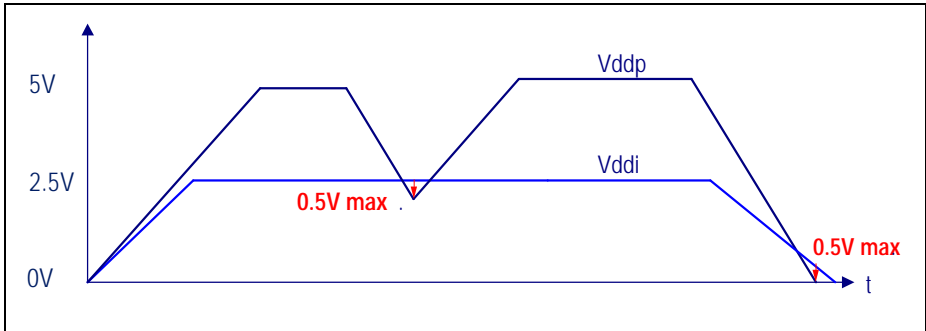


Figure 9 Dual Voltage Power Supply

Power Loss

If V_{DDP} is dropping below V_{DDI} , external circuitry in the power supply has to ensure, that V_{DDI} is also limited to the same level. If V_{DDI} is dropping below the operating range, V_{DDP} may stay active. However, again it has to be ensured, that V_{DDP} is never lower than $V_{\text{DDI}} - 0,5\text{V}$

Powering down

During powering down (falling of the supply voltages from their regular operating values to zero), it has to be ensured, that the difference between V_{DDP} and V_{DDI} ($V_{\text{DDP}} - V_{\text{DDI}}$) never drops below $- 0.5\text{V}$.

Reset Circuit

Reset must be held low until both power supplies have reached at least their respective minimum operating voltages: - $V_{\text{ddi}} = 2.35\text{V}$

$$- V_{\text{ddp}} = 4.75\text{V}$$

Reset must remain low for at least 100ns to be reliably detected (from a XTAL running state) and should remain low for at least 50ms to allow XTAL and PLL start-up (from a XTAL not running state). The RSTIN pin has no longer a built in pull up resistor, so it needs to be biased externally.

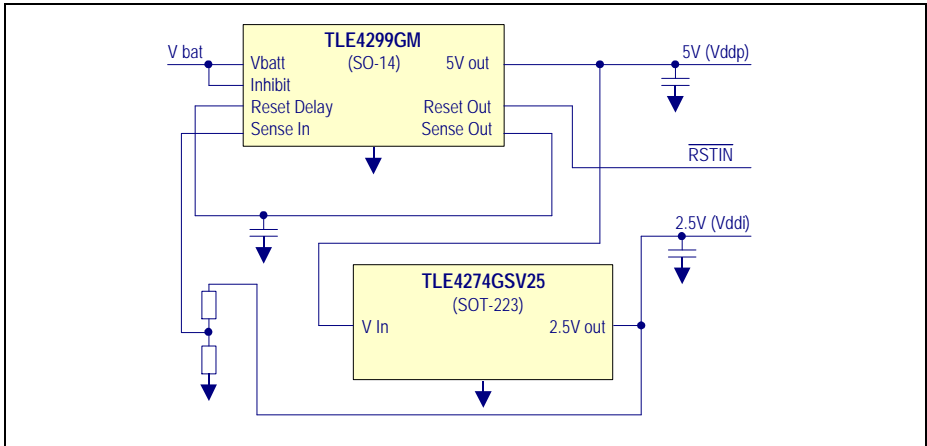


Figure 10 **Reset Circuit Discrete Component Realization**

5.3 **Oscillator**

- A new oscillator system is implemented, which has similar electrical characteristics to the C161.
- External XTAL must be in the range 4MHz to 16MHz
- Oscillator start-up time is dependent on the external circuit, and chosen safety factor, but should be 1..10ms.
- The chosen external oscillator design should be tested to ensure correct start-up and safety factor over desired temperature range.
- Before the external oscillator has started, the device runs on the base PLL frequency with a 8:1 divider, yielding 7.5 MHz to 22.5MHz.
- PLL can be set by a pre-divider, multiplier, and post divider.
- PLL can be bypassed if not required.

5.4 Debug System

On Chip Debug Support (OCDS) is implemented to provide the most important hardware emulation features to a broad range of customers at minimum cost. It allows to set breakpoints and to trace memory locations.

OCDS on chip debug features

- hardware, software and external pin breakpoints
- up to four instruction pointer breakpoints or
- masked hardware breakpoints
- support of monitor routines with programmable level
- single stepping
- trace interface through external bus (fast) or OCDS access (low end)
- read/write of GPRS/memory
- controlled via JTAG interface

The XC16x **On-Chip Emulation (OCE)** module provides functionality to the debugger in order to emulate resources and assist in application program debugging.

On-Chip Emulation features

- real time emulation
- extended trigger capability including: instruction pointer events, data events on address or value, external inputs, counters, chaining of events, timers, etc...
- software break support
- break and “break before make”
- interrupt servicing during break or monitor mode
- simple monitor mode or JTAG based debugging through instruction injection
- real time trace

5.5 Revision History

Table 8 Changes V1.0 --> V2.0

Page	Description	Notes
Page 56	Added Figure 9 Dual Voltage Power Supply	4 Dec 2002
Page 57	Added Figure 10 Reset Circuit Discrete Component Realization and Text	4 Dec 2002
Page 57	Added Chapter Oscillator	4 Dec 2002
Page 55	Added description of TLE 7469	

<http://www.infineon.com>